

General Description

The DSC2010FI1-A0021 is a high performance LVCMOS oscillator utilizing Microchip's proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality.

The DSC2010FI1-A0021 allows the user to easily modify the frequency and drive strength of the oscillator using pins.

The DSC2010FI1-A0021 has provision for up to four user-defined pre-programmed, pin-selectable output frequencies, and eight pin-selectable output drive levels to help reduce EMI.

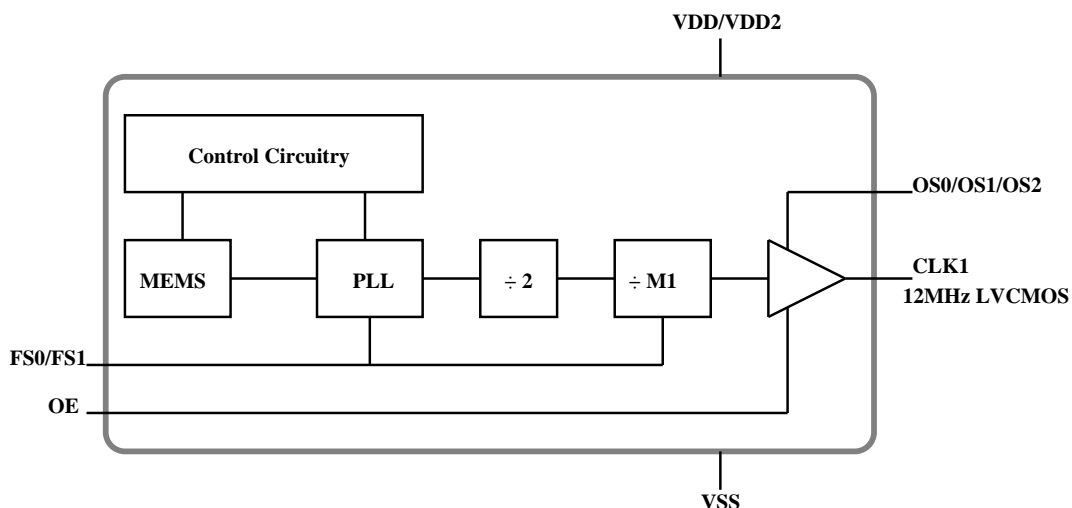
Applications

- Consumer Electronics
- Storage Area Networks
 - SATA, SAS, Fibre Channel
- Passive Optical Networks
 - EPON, 10G-EPON, GPON, 10G-GPON
- Ethernet
 - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express
- Automotive

Features

- Frequency and output formats:
 - LVCMOS
 - 12/27/25/16MHz
- Low RMS phase jitter: <1ps (typ)
- ±50ppm frequency stability
- -40°C to +85°C industrial temperature range
- High supply noise rejection: -50dBc
- Pin-selectable configurations
 - 3-bit output drive strength
 - Up to 4 output frequency combinations
- Excellent shock & vibration immunity
 - Qualified to MIL-STD-883
- High reliability
 - 20x better MTF than quartz oscillators
- Supply range of 2.25 to 3.6V
- AEC-Q100 automotive qualified
- 14-pin 3.2mm x 2.5mm QFN package

Block Diagram



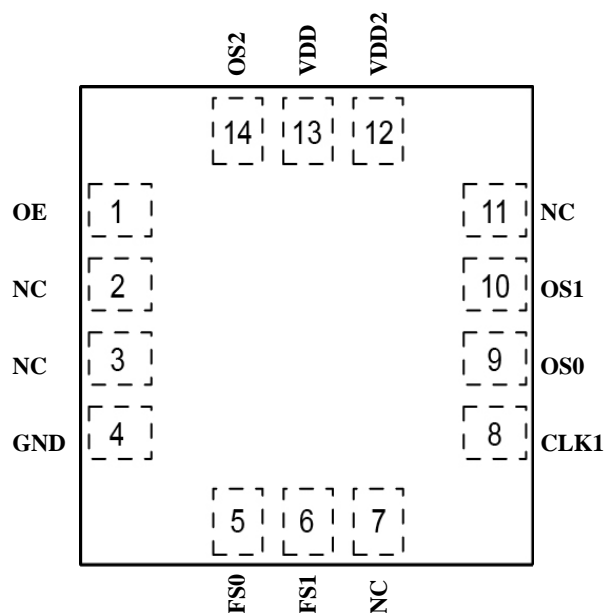
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Ordering Information

| Ordering Part Number | Industrial Temperature Range | Shipping | Package |
|----------------------|------------------------------|---------------|--------------------------|
| DSC2010FI1-A0021 | -40°C to +85°C | Tube | 14-pin 3.2mm x 2.5mm QFN |
| DSC2010FI1-A0021T | -40°C to +85°C | Tape and Reel | 14-pin 3.2mm x 2.5mm QFN |

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



14-pin 3.2mm x 2.5mm QFN

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Function |
|------------|-----------|----------|--|
| 1 | OE | I | Enables outputs when high and disables outputs when low |
| 2 | NC | | Leave unconnected or connect to ground |
| 3 | NC | | Leave unconnected or connect to ground |
| 4 | GND | PWR | Ground |
| 5 | FS0 | I | Least significant bit for frequency selection, see Table 2 for details |
| 6 | FS1 | I | Most significant bit for frequency selection, see Table 2 for details |
| 7 | NC | | Leave unconnected or connect to ground |
| 8 | CLK1 | O | LVC MOS output |
| 9 | OS0 | I | Least significant bit for output drive strength selection, see Table 1 for details |
| 10 | OS1 | I | Middle bit for output drive strength selection, see Table 1 for details |
| 11 | NC | | Leave unconnected or connect to ground |
| 12, 13 | VDD2, VDD | PWR | Power supply |
| 14 | OS2 | I | Most significant bit for output drive strength selection, see Table 1 for details |

Operational Description

The DSC2010FI1-A0021 is a LVCMOS oscillator consisting of a MEMS resonator and a supporting PLL IC. The LVCMOS output is generated through independent 8-bit programmable dividers from the output of the internal PLL.

The actual frequency output by DSC2010FI1-A0021 is controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to four different frequencies.

Two control pins (FS0, FS1) select the output frequency.

When OE (pin 1) is floated or connected to VDD, the DSC2010FI1-A0021 is in operational mode. Driving OE to ground will disable the output driver (high-impedance mode).

DSC2010FI1-A0021 has programmable output drive strength. Using three control pins (OS0-OS2) the drive strength can be adjusted to match circuit board impedances to reduce power supply noise, overshoot/undershoot and EMI. Table 1 displays typical rise / fall times for the output with a 15pF load capacitance as a function of these control pins at VDD = 3.3V and room temperature.

| | Output Drive Strength Bits [OS2, OS1, OS0] - Default is [111] | | | | | | | |
|---------|---|-----|-----|-----|-----|-----|-----|------------|
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| tr (ns) | 2.1 | 1.7 | 1.6 | 1.4 | 1.3 | 1.3 | 1.2 | 1.1 |
| tf (ns) | 2.5 | 2.4 | 2.4 | 2.2 | 1.8 | 1.6 | 1.4 | 1.4 |

Table 1. Rise/Fall Times for Drive Strengths

Output Clock Frequencies

Frequency select bits are weakly tied high so if left unconnected the default setting will be [11] and the device will output the associated frequency highlighted in bold.

| Freq (MHz) | Freq Select Bits [FS1, FS0] - Default is [11] | | | |
|------------|---|----|----|-----------|
| | 00 | 01 | 10 | 11 |
| CLK1 | 27 | 25 | 16 | 12 |

Table 2. Pin-Selectable Output Frequencies

Absolute Maximum Ratings

| Item | Min. | Max. | Units | Condition |
|----------------|------|-----------|-------|------------|
| Supply Voltage | -0.3 | +4.0 | V | |
| Input Voltage | -0.3 | VDD + 0.3 | V | |
| Junction Temp | - | +150 | °C | |
| Storage Temp | -55 | +150 | °C | |
| Soldering Temp | - | +260 | °C | 40sec max. |
| ESD | | | | |
| HBM | | 4000 | V | |
| MM | | 400 | | |
| CDM | | 1500 | | |

1000+ years of data retention on internal memory

Specifications (Unless specified otherwise: T = 25°C, max LVC MOS drive strength)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|------------------------------------|---|-----------------|--------------------|-----------------|-------|
| Supply Voltage ¹ | VDD | | 2.25 | | 3.6 | V |
| Supply Current | IDD | OE pin low - output is disabled | | 21 | 23 | mA |
| Frequency Stability | ΔF | Includes frequency variation due to initial tolerance, temp. and power supply voltage | | | ± 50 | ppm |
| Aging | ΔF | First year (@ 25°C) | | | ± 5 | ppm |
| Startup Time ² | tSU | T = 25°C | | | 5 | ms |
| Input Logic Levels Input Logic High Input Logic Low | V _{IH} V _{IL} | | 0.75 x VDD - | | - 0.25 x VDD | V |
| Output Disable Time ³ | tDA | | | | 5 | ns |
| Output Enable Time ³ | tEN | | | | 20 | ns |
| Pull-Up Resistor ⁴ | | Pull-up exists on all digital IO | | 40 | | kOhms |
| LVC MOS Output | | | | | | |
| Supply Current ⁴ | IDD | OE pin high - output is enabled CL = 15pF, F0 = 125MHz | | 31 | 35 | mA |
| Output Logic Levels Output Logic High Output Logic Low | V _{OH} V _{OL} | I = ± 6 mA | 0.9 x VDD - | | - 0.1 x VDD | V |
| Output Transition Time ³ Rise Time Fall Time | t _R t _F | 20% to 80% CL = 15pF | | 1.1 1.3 | 2 2 | ns |
| Frequency | CLK1 | [FS1, FS0] = [1, 1] | | 12 | | MHz |
| Output Duty Cycle | SYM | | 45 | | 55 | % |
| Period Jitter | JPER | F0 = 125MHz | | 3 | | psRMS |
| Integrated Phase Noise | JPH | 200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz | | 0.3 0.38 1.7 | 2 | psRMS |

Notes:

- Pin 12 VDD2, and pin 13 VDD should be filtered with 0.1uF capacitors.
- tSU is time to 100ppm stable output frequency after VDD is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Output is enabled if OE pin is floated or not connected.

Nominal Performance Parameters (Unless specified otherwise: T = 25°C, VDD = 3.3V)



Figure 1. LVC MOS Phase Jitter (integrated phase noise)

LVC MOS Output Waveform



Figure 2. LVC MOS Output Waveform

| MSL 1 @ 260°C refer to JSTD-020C | |
|-----------------------------------|--------------|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/sec Max. |
| Preheat Time 150°C to 200°C | 60 - 180 sec |
| Time maintained above 217°C | 60 - 150 sec |
| Peak Temperature | 255 - 260°C |
| Time within 5°C of actual Peak | 20 - 40 sec |
| Ramp-Down Rate | 6°C/sec Max. |
| Time 25°C to Peak Temperature | 8 min Max. |

Solder Reflow Profile

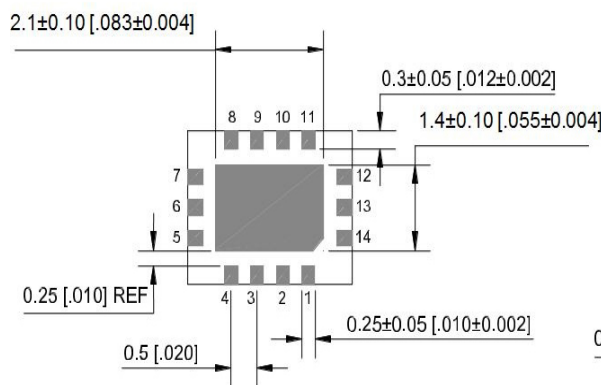
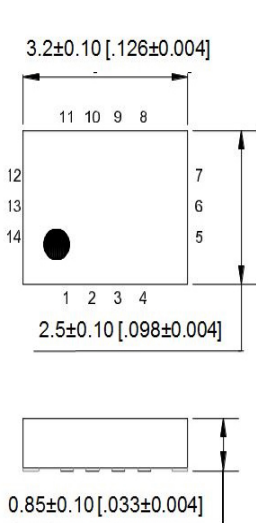


Figure 3. Solder Reflow Profile

Package Information⁶

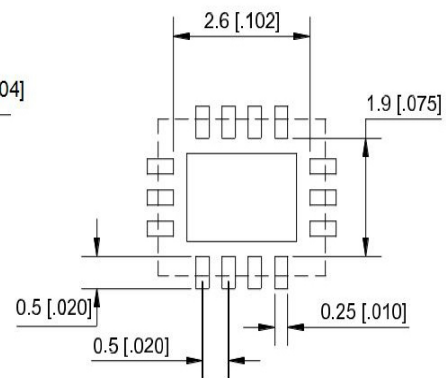
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



3.2mm x 2.5mm 14 Lead Plastic Package

Notes:

- 5. Connect the exposed die paddle to ground.
- 6. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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