DSC400-3341Q0062

Crystal-less™ Configurable Clock Generator

General Description

The DSC400-3341Q0062 is a four output crystal-less™ clock generator. It utilizes Micrel's proven PureSilicon™ MEMS technology to provide excellent jitter and stability while incorporating additional device functionality.

The frequencies of the outputs can be identical or independently derived from two shared PLLs. Each output may be configured independently to support LVCMOS, LVPECL, LVDS, or HCSL output standards.

The DSC400-3341Q0062 provides two independent select lines for choosing between two sets of pre-configured frequencies per bank. It also has two OE pins to allow for enabling and disabling outputs.

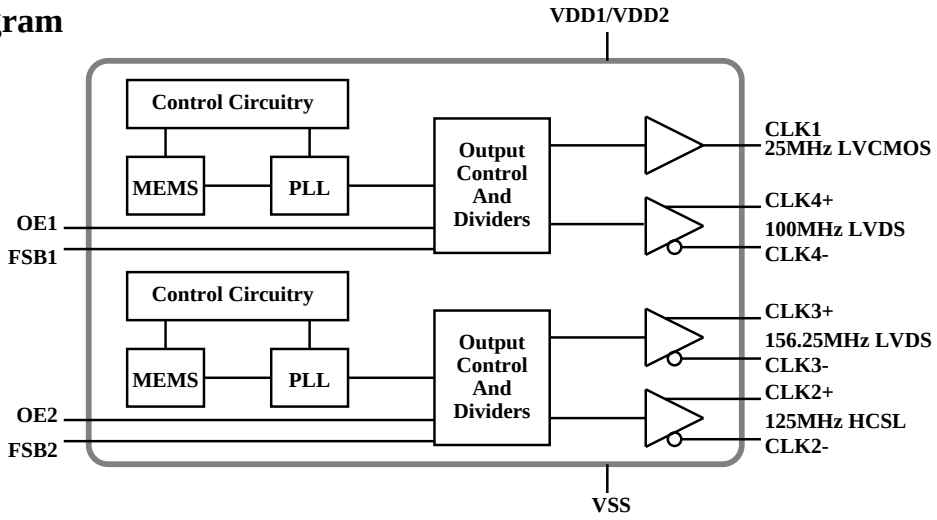
Applications

- Communications and Networks
- Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON, GPON, 10G-GPON
- HD/SD/SDI Video & Surveillance
- Automotive
- Media and Video
- Embedded and Industrial

Features

- Frequencies and output formats:
  - 25MHz LVCMOS x 1
  - 125MHz HCSL x 1
  - 156.25MHz LVDS x 1
  - 100MHz LVDS x 1
- Low RMS phase jitter: <1ps (typ)
- High stability: ±25ppm, ±50ppm
- Wide temperature range
  - Industrial: -40°C to +85°C
  - Ext. commercial: -20°C to +70°C
- High supply noise rejection: -50dBc
- Available pin-selectable frequency table
  - 1 pin per bank for 2 frequency sets
- Excellent shock & vibration immunity
  - Qualified to MIL-STD-883
- High reliability
  - 20x better MTF than quartz based devices
- Supply range of 2.25V to 3.6V
- AEC-Q100 automotive qualified
- 20-pin 5mm x 3.2mm QFN package

Block Diagram

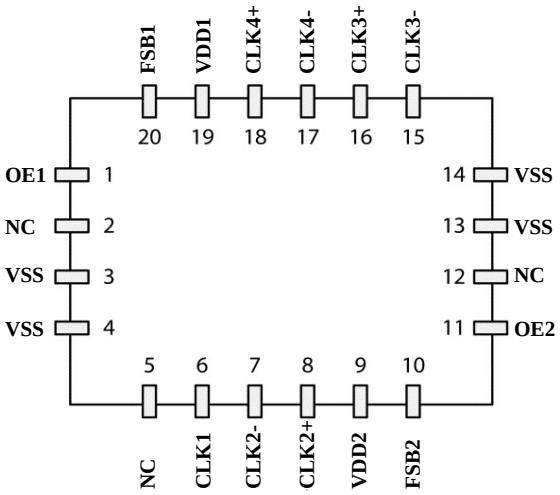


Ordering Information

Ordering Part Number	Temperature Range	High Stability	Shipping	Package
DSC400-3341Q0062KI2	-40°C to +85°C	±25ppm	Tube	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KI2T	-40°C to +85°C	±25ppm	Tape and Reel	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KI1	-40°C to +85°C	±50ppm	Tube	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KI1T	-40°C to +85°C	±50ppm	Tape and Reel	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KE2	-20°C to +70°C	±25ppm	Tube	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KE2T	-20°C to +70°C	±25ppm	Tape and Reel	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KE1	-20°C to +70°C	±50ppm	Tube	20-pin 5mm x 3.2mm QFN
DSC400-3341Q0062KE1T	-20°C to +70°C	±50ppm	Tape and Reel	20-pin 5mm x 3.2mm QFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



20-pin 5mm x 3.2mm QFN

Pin Description

Pin Number	Pin Name	Pin Type	Pin Function
1	OE1	I	Output enable for Bank 1 (CLK1 and CLK4); active high - see Table 1
2	NC		Leave unconnected or connect to ground
3	VSS	PWR	Ground
4	VSS	PWR	Ground
5	NC		Leave unconnected or connect to ground
6	CLK1	O	LVCMOS output 1 = 25MHz
7	CLK2-	O	Complement output of differential pair 2
8	CLK2+	O	True output of differential pair 2
9	VDD2	PWR	Power supply for Bank 2 (CLK3 and CLK2)
10	FSB2	I	Input for selecting pre-configured frequencies on Bank 2 (CLK3 and CLK2) No connect if the function is not used.
11	OE2	I	Output enable for Bank 2 (CLK3 and CLK2); active high - see Table 1
12	NC		Leave unconnected or connect to ground
13	VSS	PWR	Ground
14	VSS	PWR	Ground
15	CLK3-	O	Complement output of differential pair 3
16	CLK3+	O	True output of differential pair 3
17	CLK4-	O	Complement output of differential pair 4
18	CLK4+	O	True output of differential pair 4
19	VDD1	PWR	Power supply for Bank 1 (CLK1 and CLK4)
20	FSB1	I	Input for selecting pre-configured frequencies on Bank 1 (CLK1 and CLK4) No connect if the function is not used.

Operational Description

The DSC400-3341Q0062 is a crystal-less™ clock generator. Unlike older clock generators in the industry, it does not require an external crystal to operate; it relies on integrated MEMS resonators that interface with internal PLLs. This technology enhances performance and reliability by allowing tighter frequency stability over a far wider temperature range. In addition, the higher resistance to shock and vibration decreases the aging rate, greatly improving product life in the system.

Inputs

There are 4 input signals in the device. Each has an internal (40kOhms) pull up, which defaults the selection to a high (1). Inputs can be controlled through hardware strapping method with a resistor to ground to assert the input low (0). Inputs may also be controlled by other components' GPIOs. In case more than one frequency set is desired, FSB1 and FSB2 are used for independently selecting one of two sets frequency per bank. FSB1 selects the pre-configured frequency set on Bank 1 (CLK1 and CLK4) and FSB2 selects the pre-configured frequency set on Bank 2 (CLK3 and CLK2). If there is a requirement to disable outputs, the inputs OE1 and OE2 are used to disable the banks of outputs. Outputs are disabled in tristate (Hi-Z) mode, see Table 1 below.

OE1	OE2	Bank 1 (CLK1 and CLK4)	Bank 2 (CLK3 and CLK2)
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Running
1	0	Running	Hi-Z
1	1	Running	Running

Table 1. Output Enable (OE) Selection Table

Outputs

The four outputs are grouped into two banks. Each bank is supplied by an independent VDD to allow for optimized noise isolation between the two banks. Each bank provides two synchronous outputs generated by a common PLL:

- Bank 1 is composed of outputs CLK1 and CLK4
- Bank 2 is composed of outputs CLK3 and CLK2

Each output maybe pre-configured independently to be one of the following formats: LVCMOS, LVDS, LVPECL or HCSL. In case the output is configured to be single ended (LVCMOS only), the frequency is generated on the true output (CLKx+) and the complement output (CLKx-) is shut off in a low state. Frequencies can be chosen from 2.3MHz to 460MHz for differential outputs and from 2.3MHz to 170MHz on LVCMOS outputs.

Output Clock Frequencies

Output	CLK1	CLK2	CLK3	CLK4
Frequency (MHz)	25	125	156.25	100

Power

VDD1 and VDD2 supply the power to banks 1 and 2 respectively. Each VDD may have different supply voltage from the other as long as it is within the 2.25V to 3.6V range. Each VDD pin should have a 0.1µF capacitor to filter high frequency noise. VSS is common to the entire device. The exposed die paddle should be connected to VSS.

Absolute Maximum Ratings

Item	Min.	Max.	Units	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	VDD + 0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

1000+ years of data retension on internal memory

Specifications (Unless specified otherwise: Ta = 25°C, VDD = 3.3V)

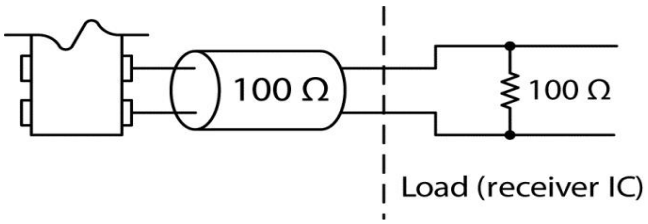
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	VDD		2.25		3.6	V
Supply Current - Core[2]	IDDcore	OE (1:2) = 0 All outputs are disabled		40	44	mA
Frequency Stability	△F	All temp and VDD ranges			±25 ±50	ppm
Aging - first year	△Fy1	1 year @ 25°C			±5	ppm
Aging - after first year	△Fy2[+]	Year 2 and beyond @ 25°C			< ±1/yr	ppm
Startup Time[3]	tSU	T = 25°C			5	ms
Input Logic Levels Input Logic High Input Logic Low	 VIH VIL		 0.75 x VDD -		 - 0.25 x VDD	V
Output Disable Time[4]	tDA	OE(1:2) transition from 1 to 0			5	ns
Output Enable Time[4]	tEN	OE(1:2) transition from 0 to 1			20	ns
Pull-Up Resistor	Rpu	All input pins have an internal pull-up		40		kOhms

Notes:

1. VDD pins should be filtered with 0.1µF capacitor connected between VDD and VSS.
2. The addition of IDDcore and IDDio provides total current consumption of the device.
3. tSU is time to 100ppm stable output frequency after VDD is applied and outputs are enabled.
4. Output Waveform figures below the parameters. See Output Waveform section.

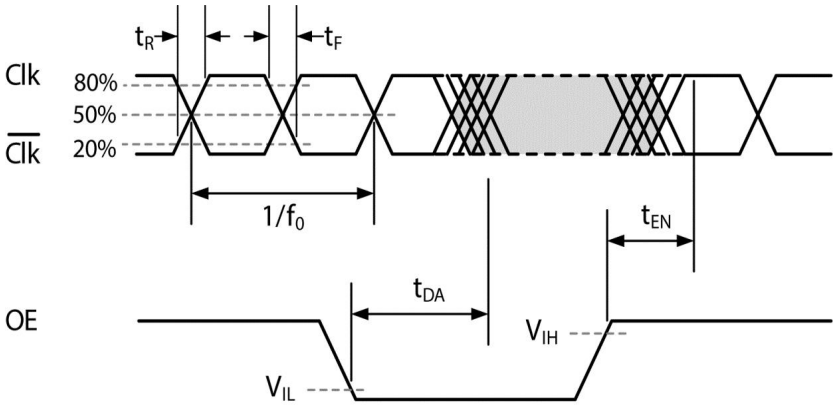
LVDS Outputs						
Output Offset Voltage	VOS	RL = 100Ohms Differential	1.125		1.4	V
Delta Offset Voltage	ΔVOS				50	mV
Pk to Pk Output Swing	VPP	Single-Ended		350		mV
Output Transition Time[3] Rise Time Fall Time	 tR tF	 20% to 80% RL = 50Ohms, CL = 2pF		 200		ps
Frequency	f3 f4	CLK3 CLK4		156.25 100		MHz
Output Duty Cycle	SYM	Differential	48		52	%
Supply Current - IO[2]	IDDio	Per output at 125MHz		9	12	mA
Period Jitter	JPER			2.5		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 156.25MHz 100kHz to 20MHz @ 156.25MHz 12kHz to 20MHz @ 156.25MHz		0.28 0.4 1.7	 2	psRMS

LVDS Typical Termination Scheme



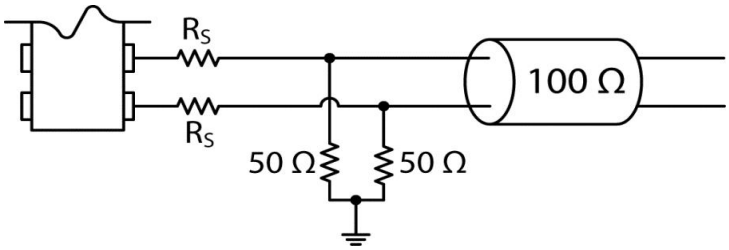
If the 100Ohms clamping resistor does not exist inside the receiving device, it should be added externally on the PCB and placed as close as possible to the receiver.

LVDS Output Waveform



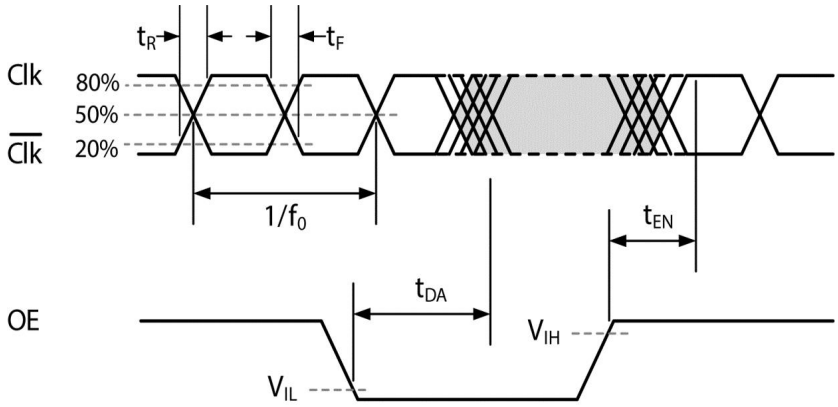
HCSL Outputs						
Output Logic Levels Output Logic High Output Logic Low	 VOH VOL	 RL = 50Ohms	 0.725 -	 	 - 0.1	V
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition Time[3] Rise Time Fall Time	 tR tF	20% to 80% RL = 50Ohms, CL = 2pF	200		400	ps
Frequency	f2	CLK2		125		MHz
Output Duty Cycle	SYM	Differential	48		52	%
Supply Current - IO[2]	IDDio	Per output at 125MHz		20	22	mA
Period Jitter	JPER			2.5		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 156.25MHz 100kHz to 20MHz @ 156.25MHz 12kHz to 20MHz @ 156.25MHz		0.25 0.37 1.7	 2	psRMS

HCSL Typical Termination Scheme



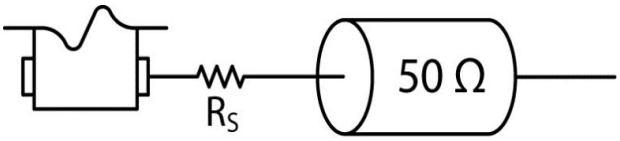
R_S is a series resistor implemented to match the trace impedance. Depending on the board layout, the value may range from 0 to 30Ohms

HCSL Output Waveform



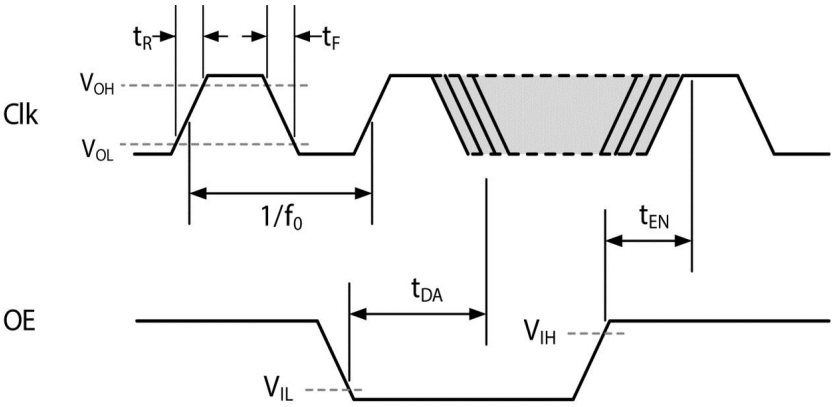
LVCMOS Outputs						
Output Logic Levels Output Logic High Output Logic Low	 VOH VOL	 I = ±6mA	 0.9 x VDD -	 	 - 0.1 x VDD	 V
Output Transition Time[3] Rise Time Fall Time	 tR tF	20% to 80% CL = 15pF		 1.1 1.3	 2 2	 ns
Frequency	f1	CLK1		25		MHz
Output Duty Cycle	SYM	Differential	45		55	%
Supply Current - IO[2]	IDDio	Per output at 125MHz, CL = 15pF		11	14	mA
Period Jitter	JPER	CLK(1:4) = 125MHz		3		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 156.25MHz 100kHz to 20MHz @ 156.25MHz 12kHz to 20MHz @ 156.25MHz		0.3 0.38 1.7	 2	psRMS

LVCMOS Typical Termination Scheme



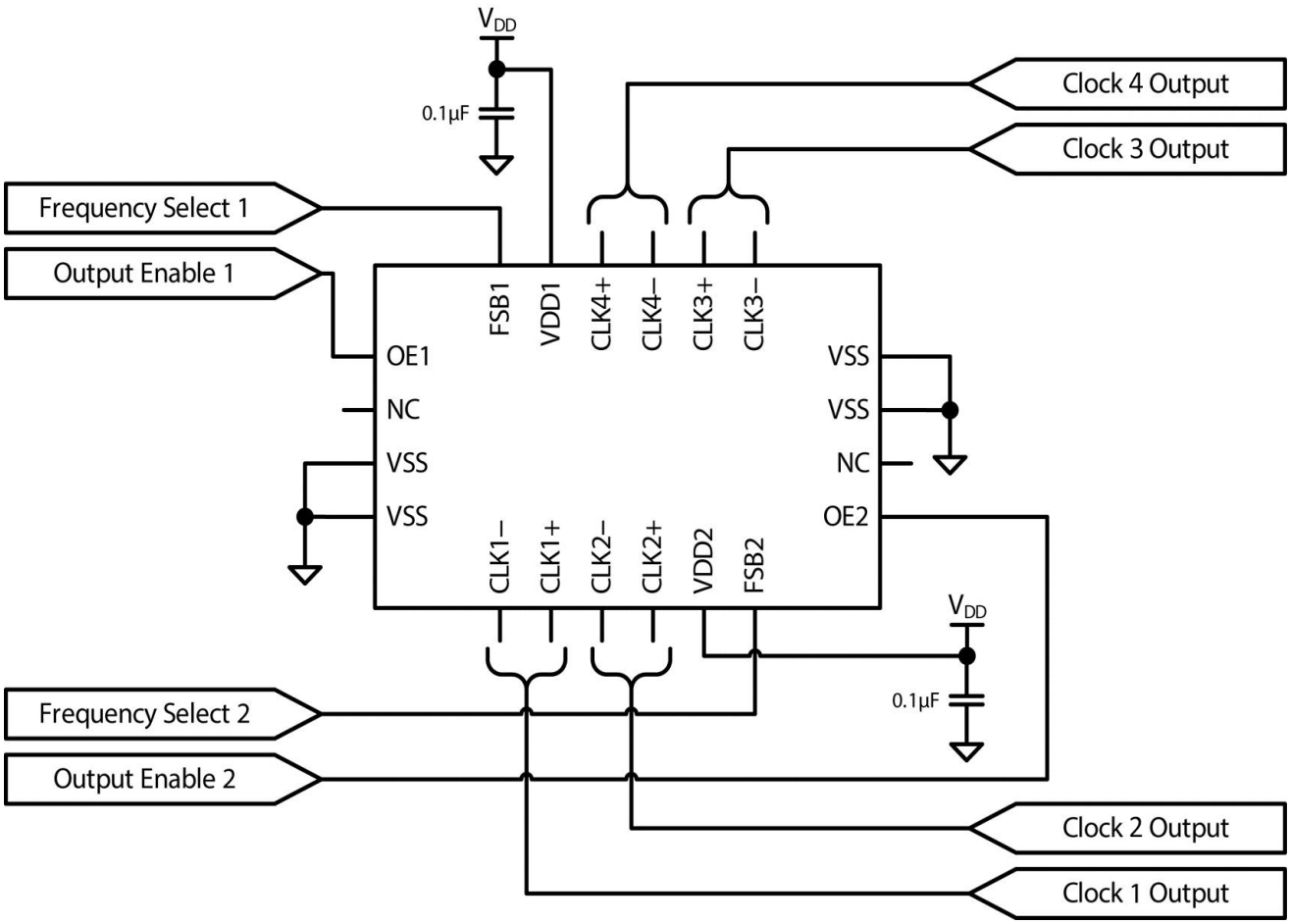
RS is a series resistor implemented to match the trace impedance to that of the clock output. Depending on the board layout, the value may range from 0 to 27Ohms.

LVCMOS Output Waveform

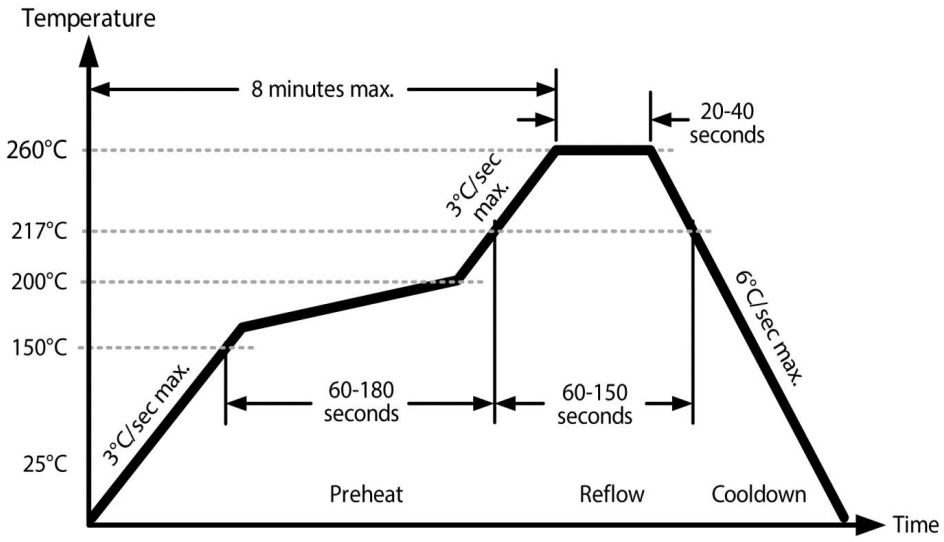


Connection Diagram

The connection Diagram below includes recommended capacitors to be placed on each VDD for noise filtering.

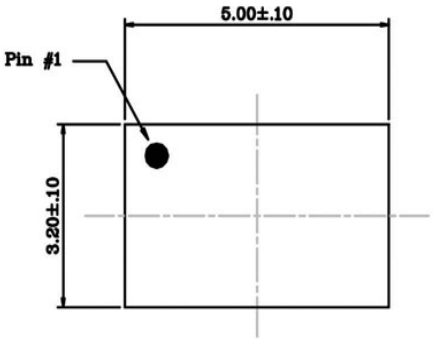


Solder Reflow Profile

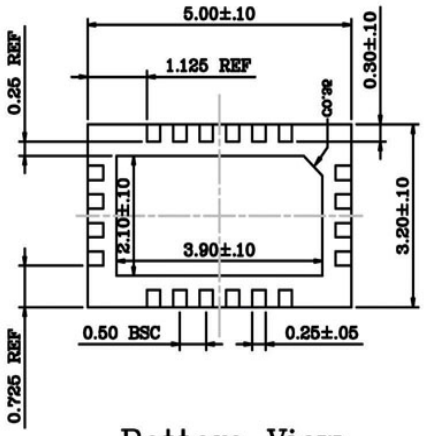


MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec Max.
Preheat Time 150°C to 200°C	60 - 180 sec
Time maintained above 217°C	60 - 150 sec
Peak Temperature	255 - 260°C
Time within 5°C of actual Peak	20 - 40 sec
Ramp-Down Rate	6°C/sec Max.
Time 25°C to Peak Temperature	8 min Max.

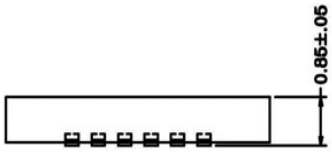
Package Information



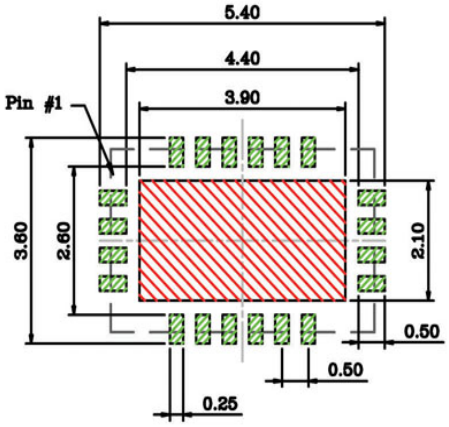
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep-out area.

20 QFN, 5.0mm x 3.2mm Package

Recommended Solder Pad layout

Connect the center pad to ground plane for best thermal performance.