SM802123

Flexible Ultra-Low Jitter Clock Generator

ClockWorks® FLEX

General Description

The SM802123 is a member of the ClockWorks® FLEX family of devices from Microchip and provides an extremely low-noise timing solution. It is based upon a unique PLL architecture that provides very-low phase noise.

The device operates from a 2.5V or 3.3V power supply.

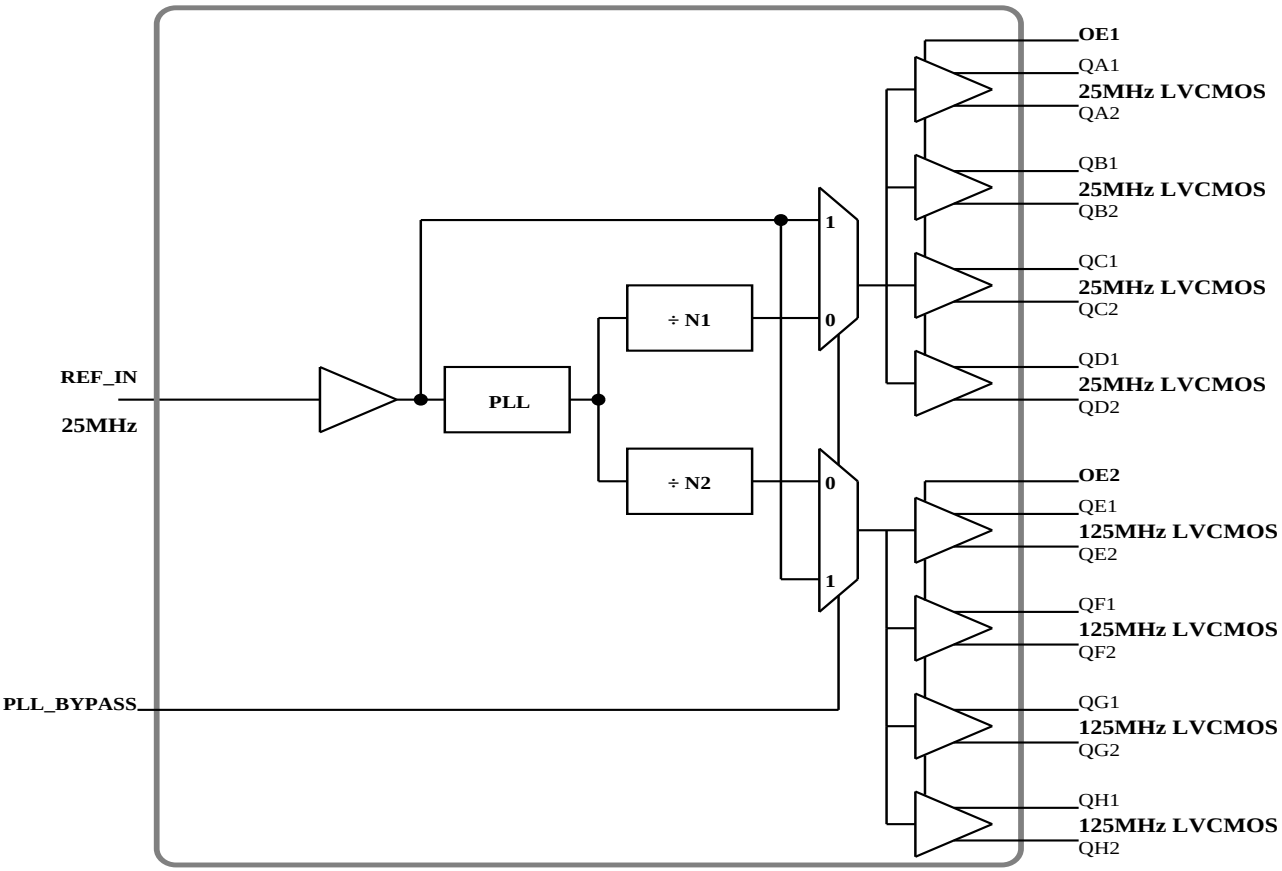
Applications

- Gigabit Ethernet
- Storage

Features

- Generates 16 output clocks
- Frequency and output logic:
  - 25MHz LVCMOS x 8
  - 125MHz LVCMOS x 8
- 25MHz Reference Input
- OE on banks 1 and 2
- PLL_Bypass mode
- Typical phase noise:
  - 260fs (Integration range: 12kHz-20MHz)
- On-chip power supply regulation for excellent board level power supply noise immunity
- No external crystal oscillator capacitors required
- 2.5V or 3.3V operating power supply
- Industrial temperature range
- 44-Pin 7mm x 7mm QFN package

Block Diagram

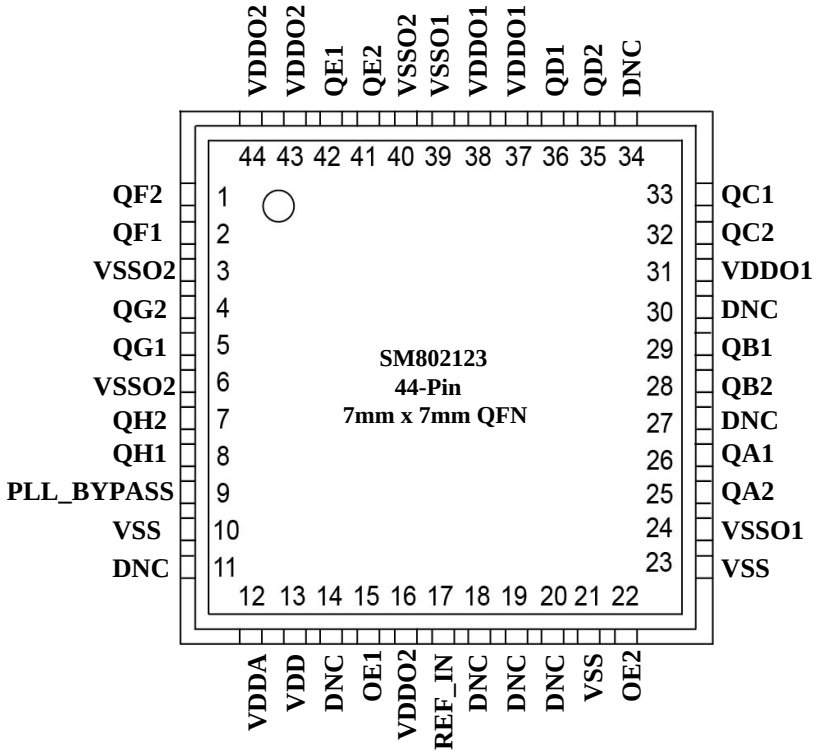


Ordering Information

Ordering Part Number	Marking	Shipping	Ambient Temperature Range	Package
SM802123UMG	802123	Tray	-40°C to +85°C	44-Pin QFN (7x7 mm)
SM802123UMG TR	802123	Tape and Reel	-40°C to +85°C	44-Pin QFN (7x7 mm)

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1, 2	QF2, QF1	O, SE	LVCMOS (0°, 0°)	Bank 2 Clock Output Frequency = 125MHz
3, 6, 40	VSS02	PWR		Power Supply Ground for the Outputs on Bank 2
4, 5	QG2, QG1	O, SE	LVCMOS (0°, 0°)	Bank 2 Clock Output Frequency = 125MHz
7, 8	QH2, QH1	O, SE	LVCMOS (0°, 0°)	Bank 2 Clock Output Frequency = 125MHz
9	PLL_BYPASS	I, SE	LVCMOS	Bypass the PLL and switches the XTAL or REF_IN frequency to all outputs. 0 = PLL Mode, 1 = Bypass Mode, 45k Ohms Pull-Down
10, 21, 23	VSS	PWR		Core Power Supply Ground
11, 20, 27, 30, 34	DNC			Do not connect anything to these pins.
12	VDDA	PWR		Analog Power Supply
13	VDD	PWR		Core Power Supply
14	DNC			Do not connect
15	OE1	I, SE	LVCMOS	Output Enable, Bank 1 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45k Ohms Pull-Up
16, 43, 44	VDDO2	PWR		Power Supply for the Outputs on Bank 2
17	REF_IN	I, SE	LVCMOS	Reference Input = 25MHz
18, 19	DNC			Do not connect
22	OE2	I, SE	LVCMOS	Output Enable, Bank 2 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45k Ohms Pull-Up
24, 39	VSS01	PWR		Power Supply Ground for the Outputs on Bank 1
25, 26	QA2, QA1	O, SE	LVCMOS (0°, 0°)	Bank 1 Clock Output Frequency = 25MHz
28, 29	QB2, QB1	O, SE	LVCMOS (0°, 0°)	Bank 1 Clock Output Frequency = 25MHz
31, 37, 38	VDDO1	PWR		Power Supply for the Outputs on Bank 1
32, 33	QC2, QC1	O, SE	LVCMOS (0°, 0°)	Bank 1 Clock Output Frequency = 25MHz
35, 36	QD2, QD1	O, SE	LVCMOS (0°, 0°)	Bank 1 Clock Output Frequency = 25MHz
41, 42	QE2, QE1	O, SE	LVCMOS (0°, 0°)	Bank 2 Clock Output Frequency = 125MHz
-	EXPOSED PAD	-		The exposed pad must be connected to the VSS ground plane.

Absolute Maximum Ratings[1]

Supply Voltage (VDD, VDDO1, VDDO2).....+4.6V
Input Voltage (VIN).....-0.50V to VDD + 0.5V
Lead Temperature (soldering, 20s).....260°C
Case Temperature.....115°C
Storage Temperature (T_S).....-65°C to +150°C
ESD Machine Model.....200V
ESD Human Body Model.....2000V

Operating Ratings[2]

Supply Voltage (VDD, VDDO1, VDDO2)
.....2.375V to +3.465V
Ambient Temperature (TA).....-40°C to +85°C
Junction Thermal Resistance[3]
QFN (T_{JA}) Still Air.....24°C/W

DC Electrical Characteristics[4]

VDD = VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VDD, VDDO1, VDDO2	3.3V Operating Voltage 2.5V Operating Voltage	VDDO1 = VDDO2 VDDO1 = VDDO2	3.135 2.375	3.3 2.5	3.465 2.625	V
IDD	Total supply current, VDD + VDDO	Outputs unterminated			122	mA

LVCMOS Inputs DC Electrical Characteristics[4] (REF_IN, PLL_BYPASS, OE1, OE2)

VDD = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VIH	Input High Voltage		2		VDD + 0.3	V
VIL	Input Low Voltage		-0.3		0.8	V
IIH	Input High Current	VDD = VIN = 3.465V			150	µA
IIL	Input Low Current	VDD = 3.465V, VIN = 0V	-150			µA

REF_IN DC Electrical Characteristics[4]

VDD = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VIH	Input High Voltage		1.1		VDD + 0.3	V
VIL	Input Low Voltage		-0.3		0.6	V
IIN	Input Current	XTAL_SEL = VIL, VIN = 0V to VDD XTAL_SEL = VIH, VIN = VDD	-5	 20	5	µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

LVCMOS DC Electrical Characteristics[4]

VDD = VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C, RL = 50 Ohms to VDDO/2

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Output High Voltage	Figure "LVCMOS Output Load and Test Circuit"	VDDO - 0.7			V
VOL	Output Low Voltage	Figure "LVCMOS Output Load and Test Circuit"			0.6	V

AC Electrical Characteristics[4]

VDDA = VDD = 3.3V ±5% or 2.5V ±5%
VDDO = 2.5V or 3.3V ±5%
TA = -40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
FIN	Input Frequency	Reference Input		25		MHz
FOUT	Output Frequency	Bank 1 Bank 2		25 125		MHz
TR/TF	Output Rise/Fall time	20% - 80% LVCMOS ouput	100		500	ps
ODC	Output Duty Cycle	<350MHz output frequencies	48	50	52	%
Tskew	Output-to-Output Skew	Note 5			60	ps
Tlock	PLL Lock Time				20	ms
Tjit(Ø)	RMS Phase Noise	Note 6 25MHz LVCMOS: Integration range (1kHz-5MHz) Integration range (12kHz-5MHz)		 264 260		fs

Notes:

5. Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system. Reference frequency generated using R+S SMA100A (option 02). When using an external reference input, use a low phase noise source as the phase noise will follow the input source phase noise up to about 1MHz.

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF below) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the SM802xxx.

The impedance value of the Ferrite Bead (FB) needs needs to be between 80 Ohms and 240 Ohms with a saturation current >=250mA.

The VDDO1 and VDDO2 pins connect directly to the VDD Plane. All VDD pins on the SM802xxx connect to VDD after the power supply filter.

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces.

For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Filtering Recommendations

Preferred filter, using Microchip MIC94325 Ripple Blocker:

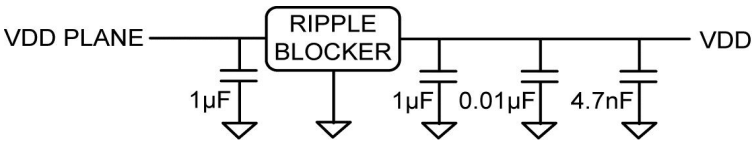


Figure 1. Vdd filter using Microchip MIC94325 Ripple Blocker

Alternative, traditional filter, using a ferrite bead:

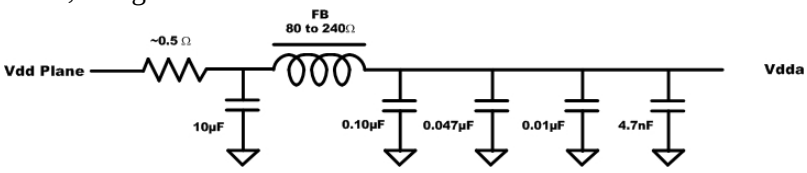


Figure 2. VDDA (Analog) traditional Pi filter

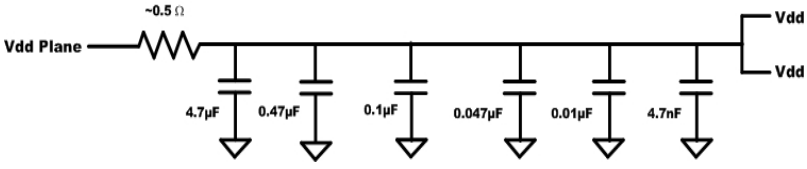


Figure 3. Recommended Power Supply Filtering

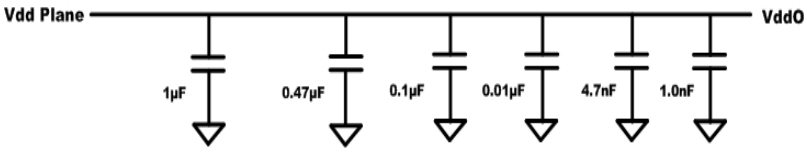


Figure 4. Recommended decoupling for each VDDO

Timing Diagrams

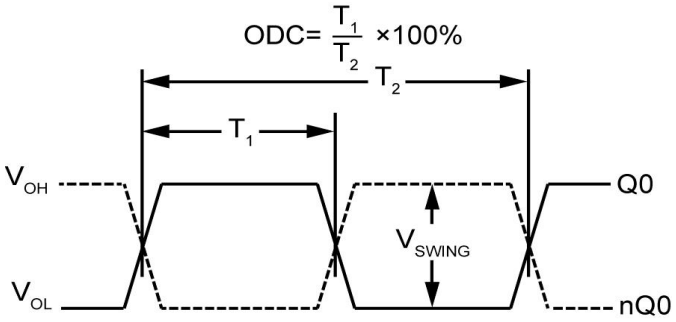


Figure 5. Duty Cycle Timing

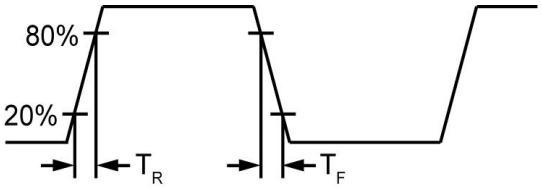


Figure 6. All Outputs Rise/Fall Time

RMS Phase/Noise/Jitter

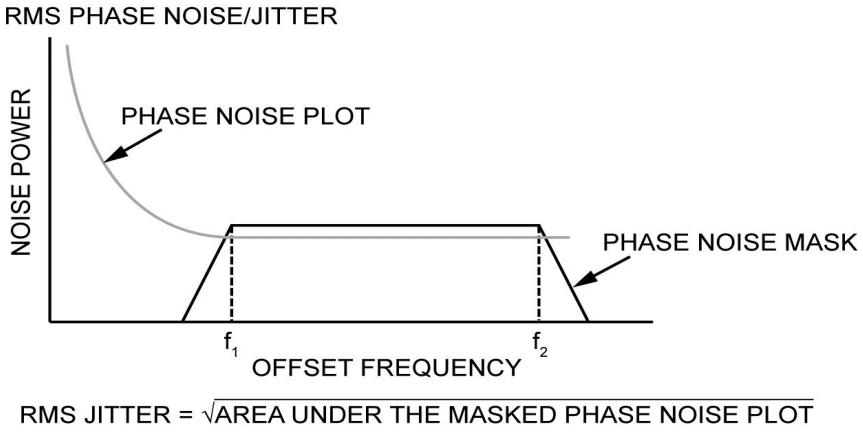


Figure 7. RMS Phase/Noise/Jitter

Output Termination

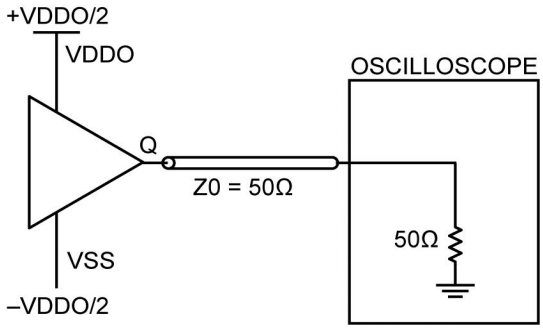


Figure 8. LVCMOS Output Load and Test Circuit

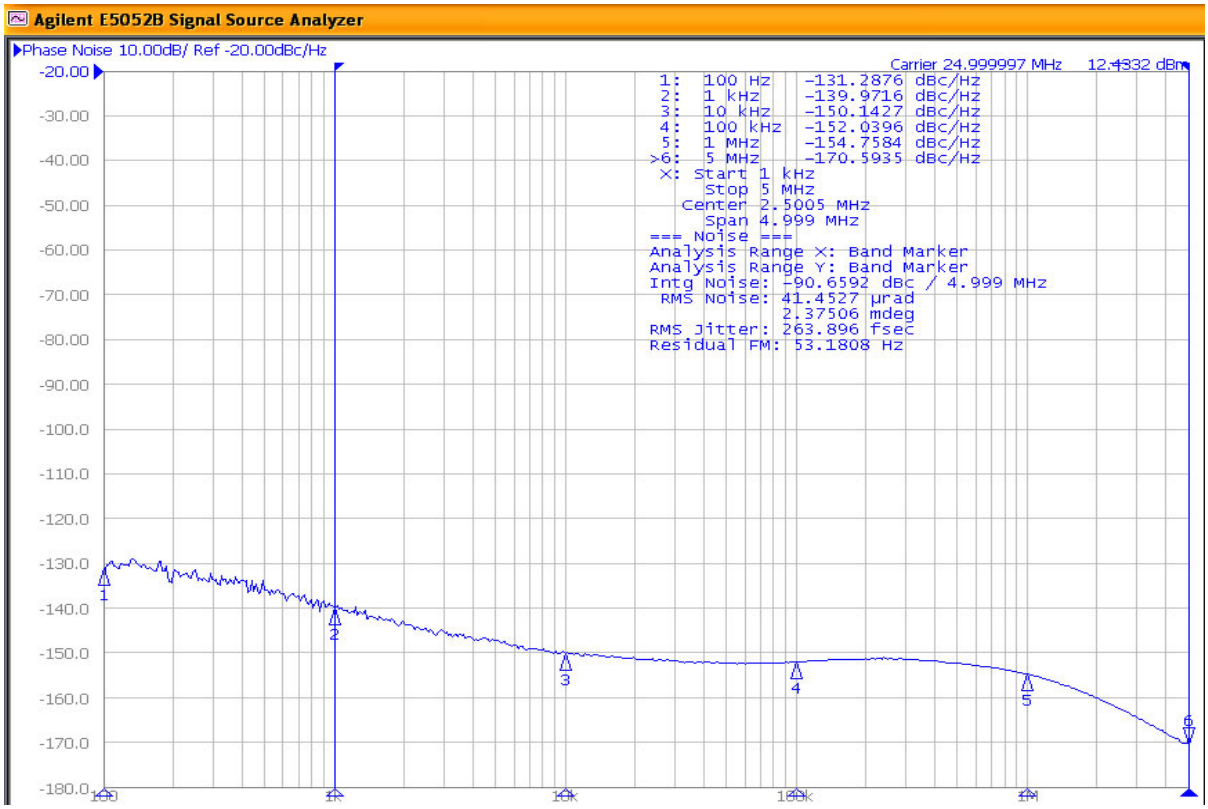


Figure 9. External Clock: 25MHz LVCMOS Output 1kHz-5MHz 264fs

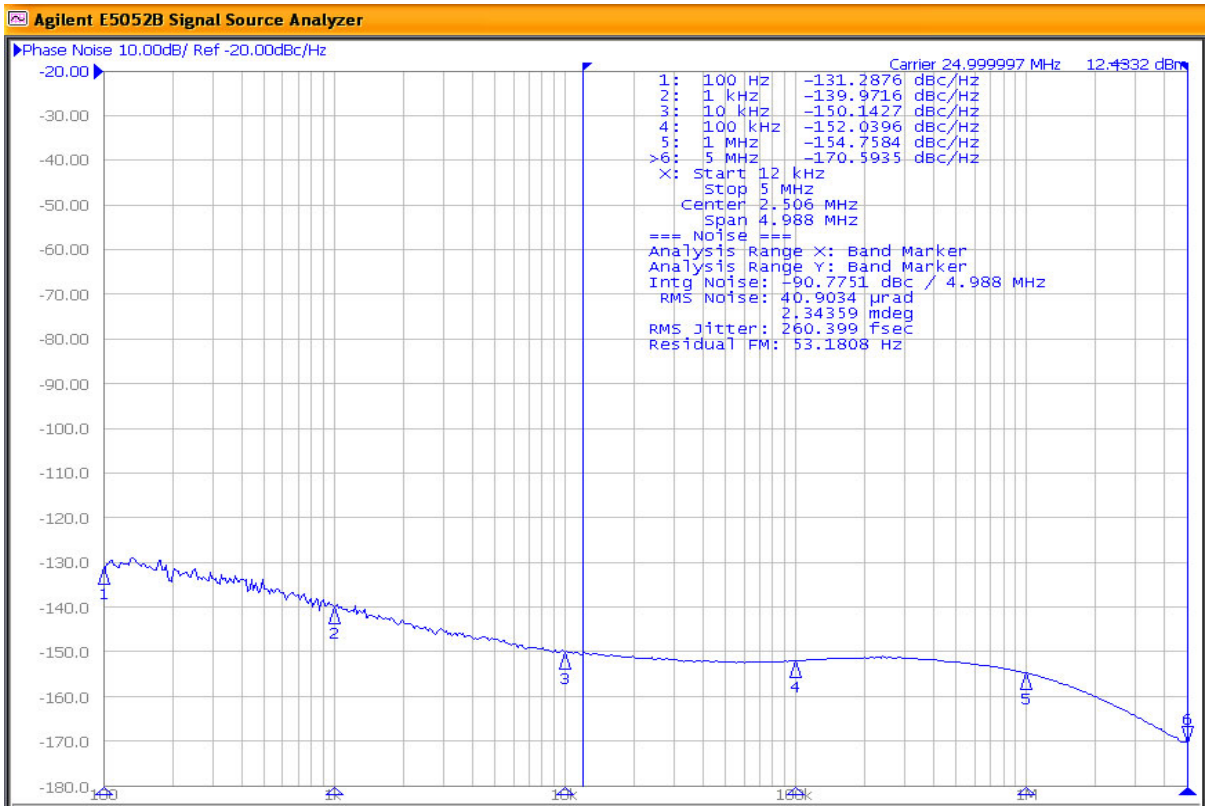


Figure 10. External Clock: 25MHz LVCMOS Output 12kHz-5MHz 260fs

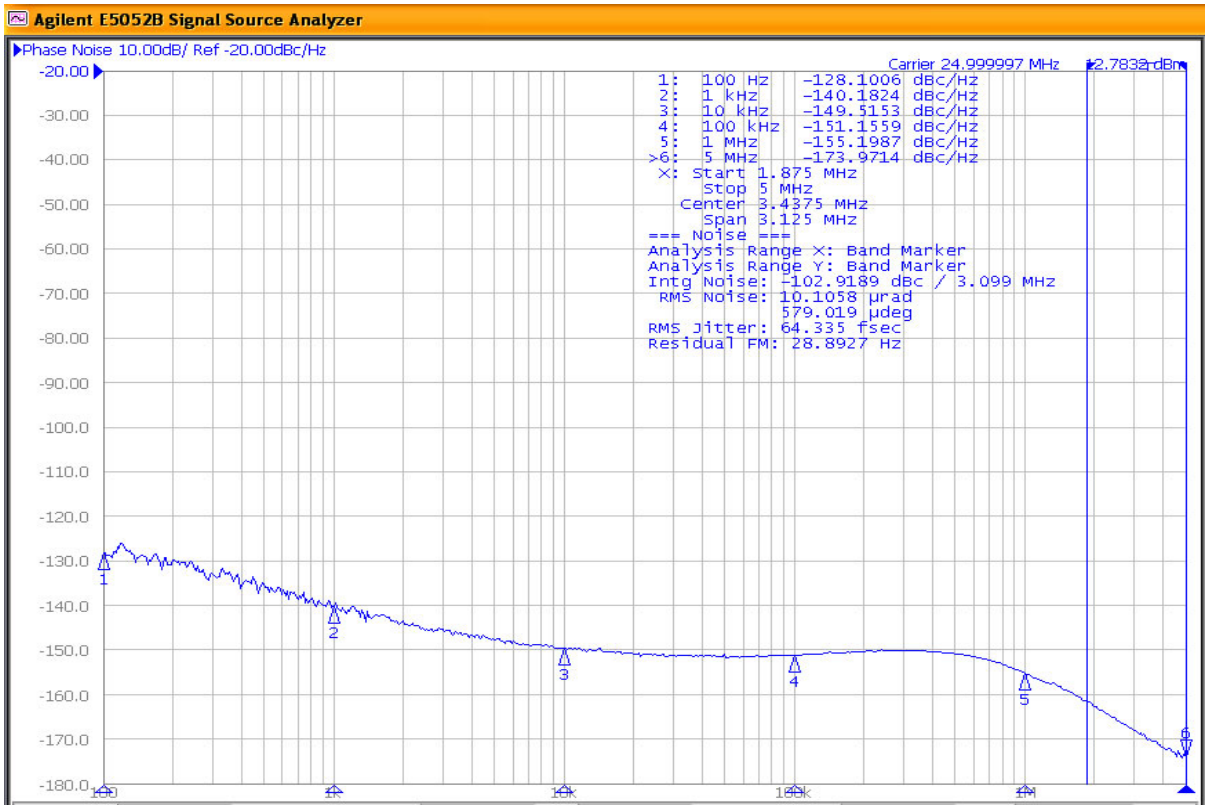


Figure 11. 25MHz LVCMOS Output 1.875MHz-5MHz 64fs

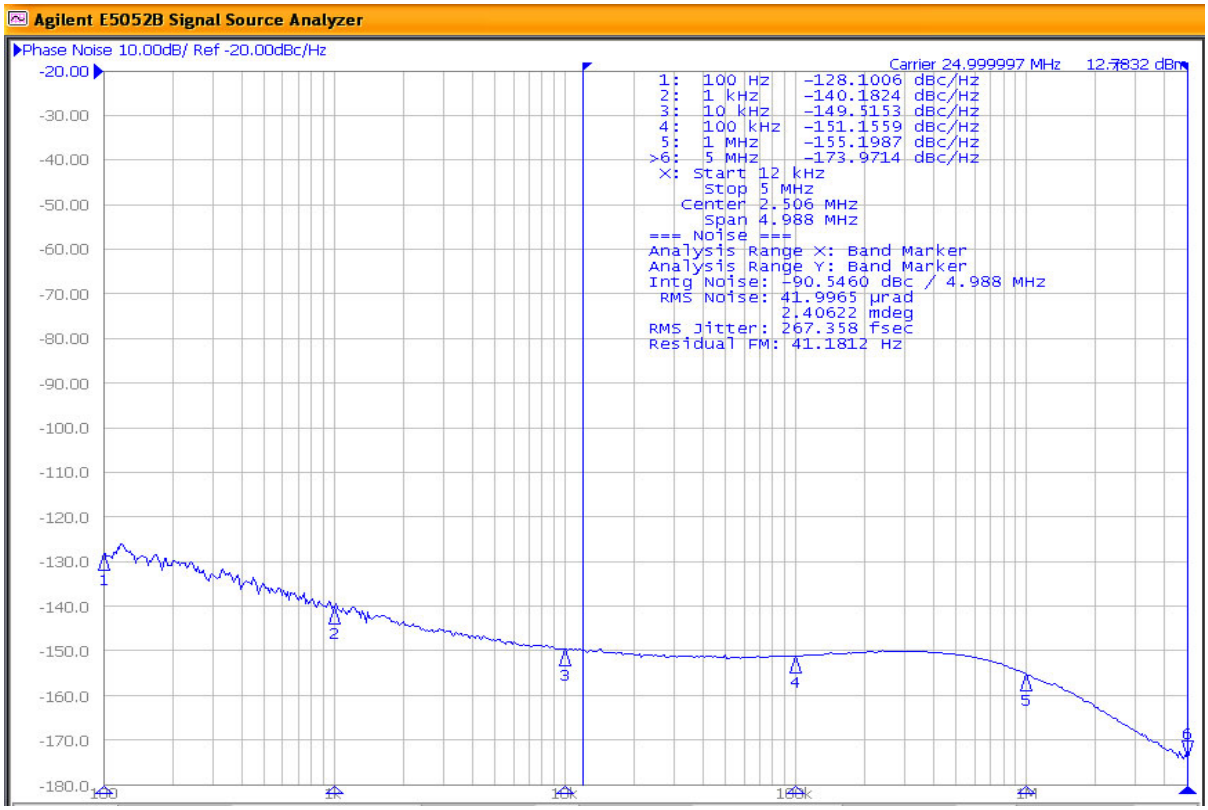
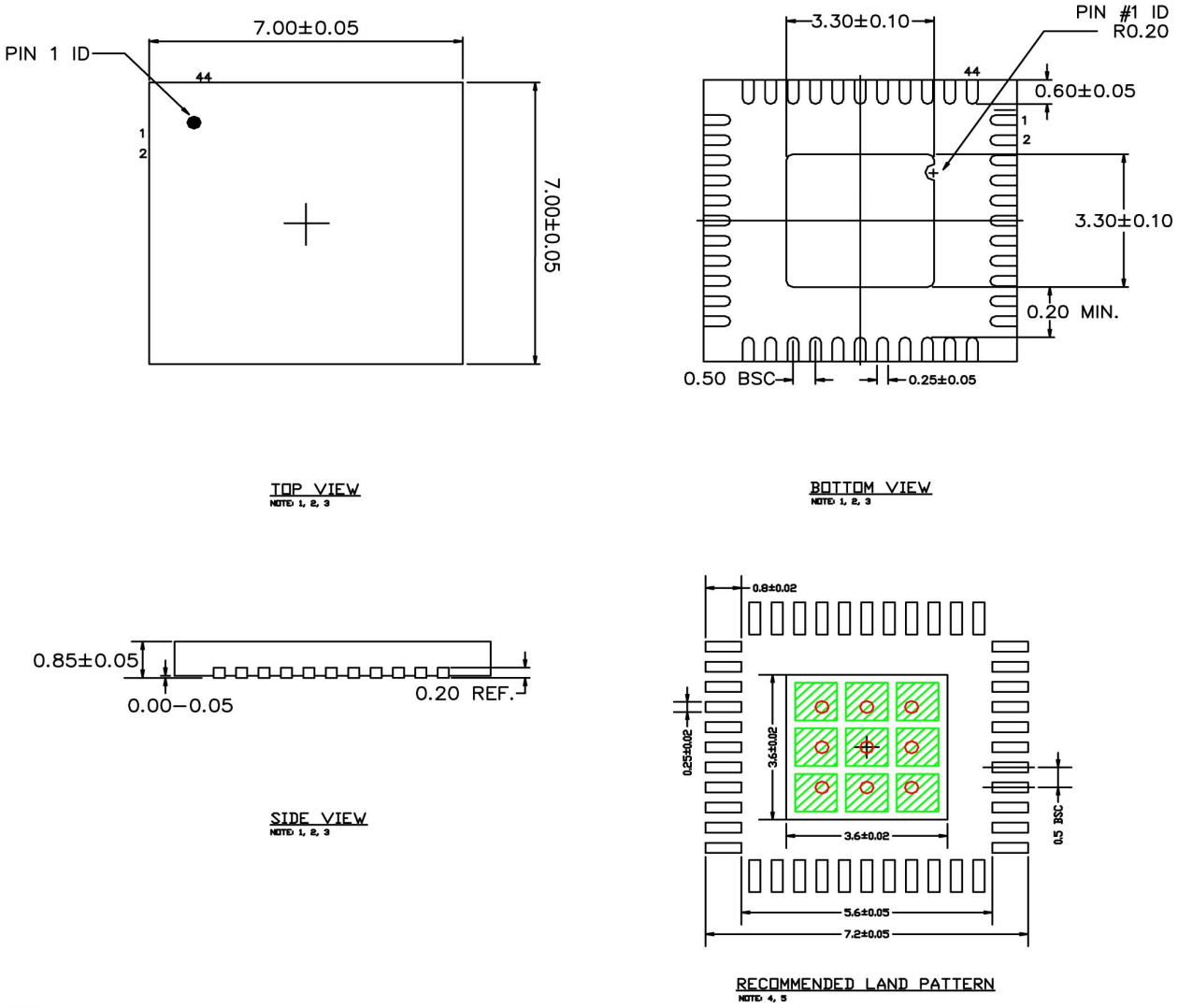


Figure 12. 25MHz LVCMOS Output 12kHz-5MHz 267fs

Package Information and Recommended Land Pattern for 44-Pin QFN[7]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30−0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.0MM PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93x0.93MM, SPACING IS 0.2MM

44-Pin QFN (7x7 mm)

Note:

7. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.