SM803115

Ultra-Low Jitter Clock Synthesizer

Preliminary Rev.0.03 04/08/14

General Description

The SM803115 is a high performance clock synthesizer featuring high integration that provides multiple frequencies from a single 50MHz low cost crystal. With ultra-low jitter performance, this IC meets the requirements of a broad range of communications protocols and chipset ICs.

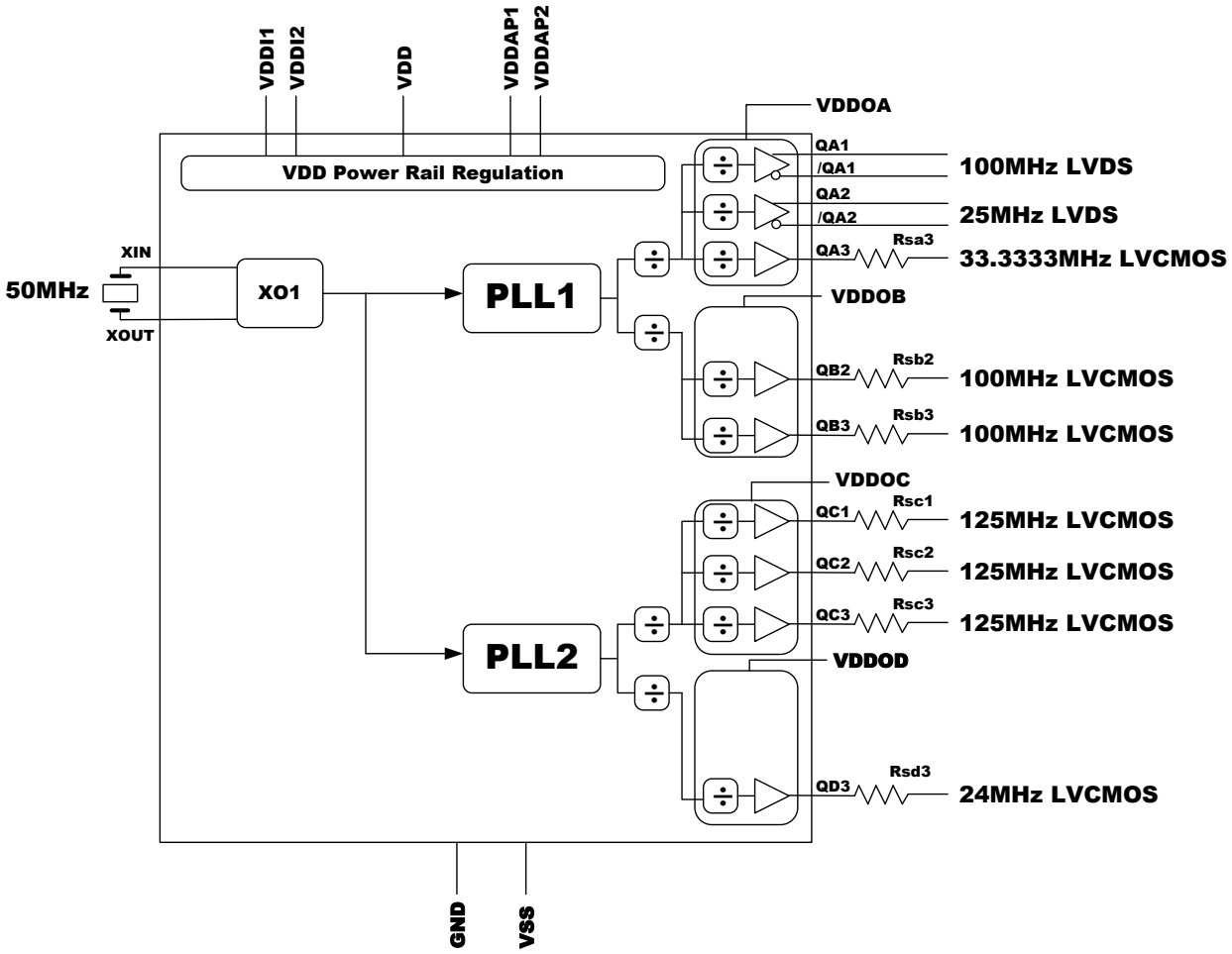
Features

- Multi-output generates all clocks from single IC
- Ultra-low jitter performance

Applications

- Ethernet switches
- Servers, line cards, telecommunications systems

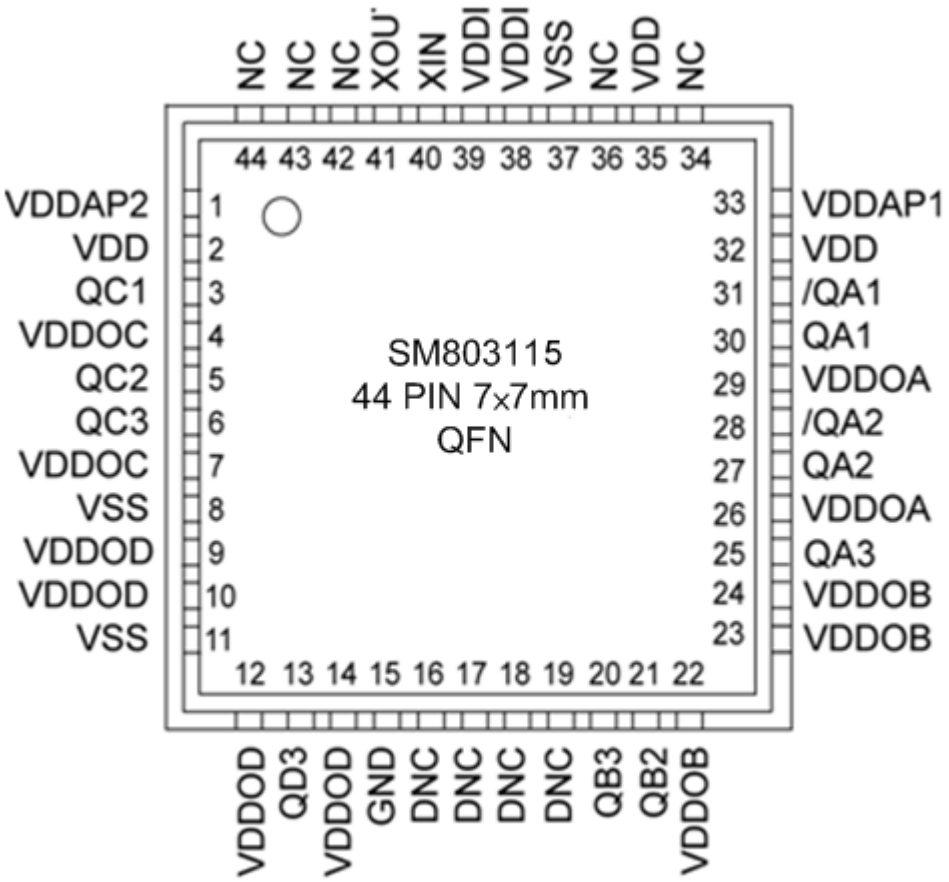
Block Diagram



Ordering Information

Part Number	Marking	Ambient Temp. Range	Package
SM803115UMG	803115	–40° to +85°C	Bulk
SM803115UMG TR	803115	–40° to +85°C	Tape and Reel

Pin Configuration



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Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
30, 31 27, 28 25 21 20 3 5 6 13	QA1, /QA1 QA2, /QA2 QA3 QB2 QB3 QC1 QC2 QC3 QD3	O, (DIF/SE)	LVDS *LVCMOS (Q only)	Differential/*SE Clock Output
2, 32, 35	VDD	PWR		Power Supply
26, 29	VDDOA	PWR		Power Supply for Outputs QA1, QA2 and QA3
22, 23, 24	VDDOB	PWR		Power Supply for Outputs QB2 and QB3
4, 7	VDDOC	PWR		Power Supply for Outputs QC1, QC2 and QC3
9, 10, 12, 14	VDDOD	PWR		Power Supply for Output QD3
33	VDDAP1	PWR		Power Supply for PLL1
1	VDDAP2	PWR		Power Supply for PLL2
38 39	VDDI1 VDDI2	PWR	3.3V only	Power Supply for XO
8, 11, 37	VSS (Exposed Pad)	PWR		Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
15	GND	I, (SE)	-	This pin is not a power supply ground but MUST be tied to VSS.
34, 36, 42, 43, 44	NC			No Connect Leave open or connect to VSS
16, 17, 18, 19	DNC			Do Not Connect (leave open).
40	XIN	I, (SE)	*12pF crystal	Crystal Reference Input, no load caps needed (see Figure 6).
41	XOUT	O, (SE)	*12pF crystal	Crystal Reference Output, no load caps needed (see Figure 6).

Absolute Maximum Ratings[1]

Supply Voltage ($V_{DD,}$ V_{DDA}, V_{DDI}, V_{DDO}) .....+4.6V
Input Voltage (V_{IN}).....-0.50V to 4.6V
Lead Temperature (soldering, #sec.)..... 260°C
Storage Temperature (T_s) .....-65°C to +150°C
ESD Machine Model 200V

Operating Ratings[2]

Supply Voltage ($V_{DD,}$ V_{DDO})..... +2.375V to +3.465V
Ambient Temperature (T_A) .....–40°C to +85°C
Junction Thermal Resistance
QFN (T_{JA}) Still Air.....24°C/W

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.

Electrical Characteristics

Typical values are T_A = 25°C, min/max across –40°C≤ T_A ≤ +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}, V_{DDO}	Supply voltage	2.5V Operation	2.375	2.5	2.625	V
		3.3V Operation	3.135	3.3	3.465	V
V_{DDI1}	Analog supply voltage		3.135	3.3	3.465	V
V_{DDI2}	Analog supply voltage		2.375		3.465	V
V_{DDA}	PLL core voltage		2.375		3.465	V
I_{DDA}	PLL core current consumption	Per active PLL			60	mA
I_{DDI}	Analog Current consumption				8	mA
I_{DDO}	Output stage current consumption	Per output bank, unloaded			70	mA

LVDS DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	Figure 1, 4	245	350	454	mV
V_{CM}	Common Mode Voltage		1.125	1.2	1.375	V
V_{OH}	Output High Voltage		1.248	1.375	1.602	V
V_{OL}	Output Low Voltage		0.898	1.025	1.252	V

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LVCMOS DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage		VDD-0.8			V
V_{OL}	Output Low Voltage				0.5	V
V_{IH}	Input High Voltage		V_{DD0} - 0.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		VSS-0.3		0.3*VDD	V
I_{IH}	Input High Current	VDD = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load Typical, Figure 6	**Fundamental, Parallel Resonant**			
Frequency			50		MHz
Frequency stability	Total stability, inclusive of: • Room temperature accuracy • Temp. drift, -5°C ~ +50°C • Aging up to 10 years	-40		+40	ppm
Equivalent Series Resistance (ESR)				60	Ω
Shunt Capacitor, C0			2	4	pF
Correlation Drive Level			10	100	uW

AC Electrical Characteristics

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

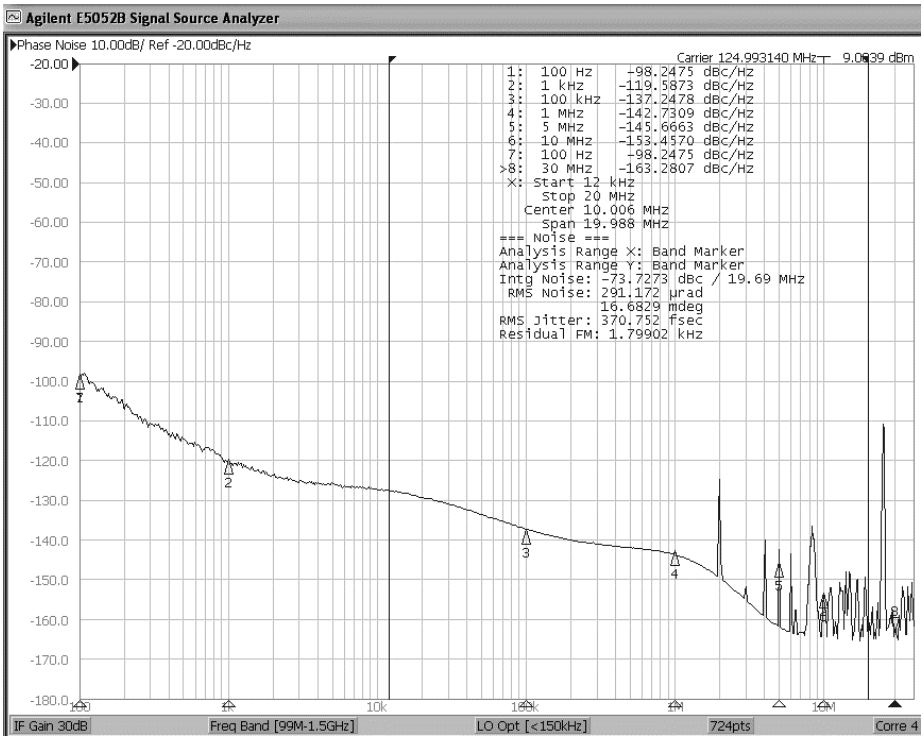
T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_R/T_F	Output Rise/Fall Time	LVDS output, Figure 2, 4	85	140	300	ps
		LVCMOS output, Figure 2, 5	100	200	400	ps
ODC	Output Duty Cycle		45	50	552	%
T_{SKEW}	Output-to-Output Skew[2]	Same output bank	-50		50	ps
T_{LOCK}	PLL Lock Time			5	20	ms
T_{jit}(∅)	Typical RMS Phase Jitter[1]	Integration Range (12kHz – 20MHz)		250		fs
dF	Frequency stability	Outputs total stability, T_A = -5°C ~ +50°C	-50		+50	ppm
T_{RAMP}	VDD Ramp Up Speed requirement	For VDD < 2.25V	+1.0			V/ms

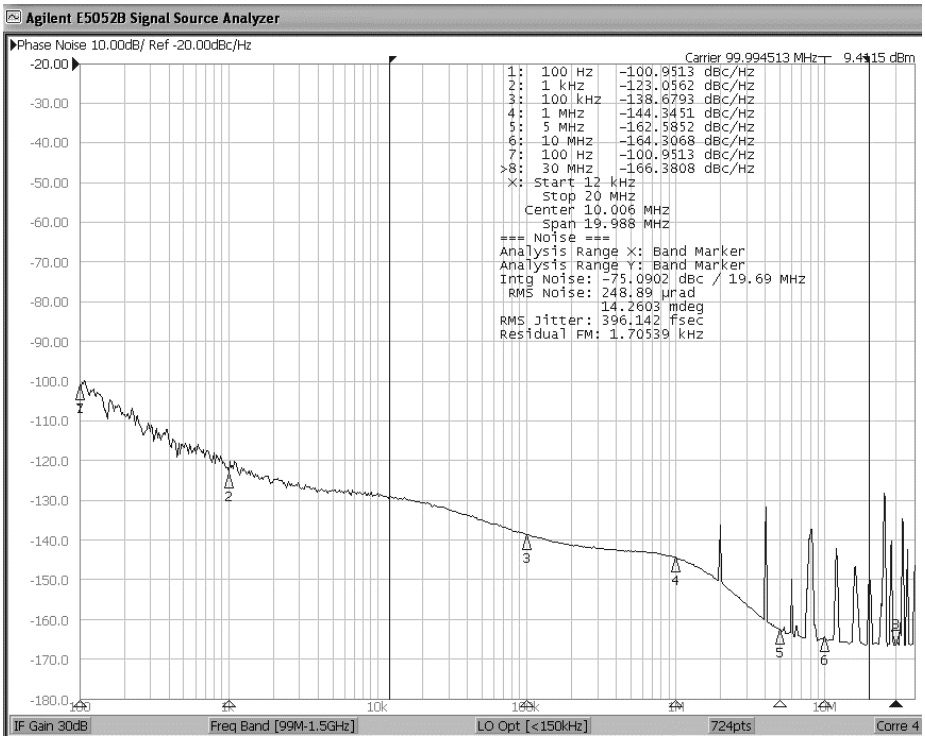
Notes:

1. All phase noise measurements were taken with an Agilent 5052B phase noise system.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.

Phase Noise



125MHz LVCMOS: 0.37ps Phase Jitter for 12KHz to 20MHz



100MHz LVCMOS: 0.40ps Phase Jitter for 12KHz to 20MHz

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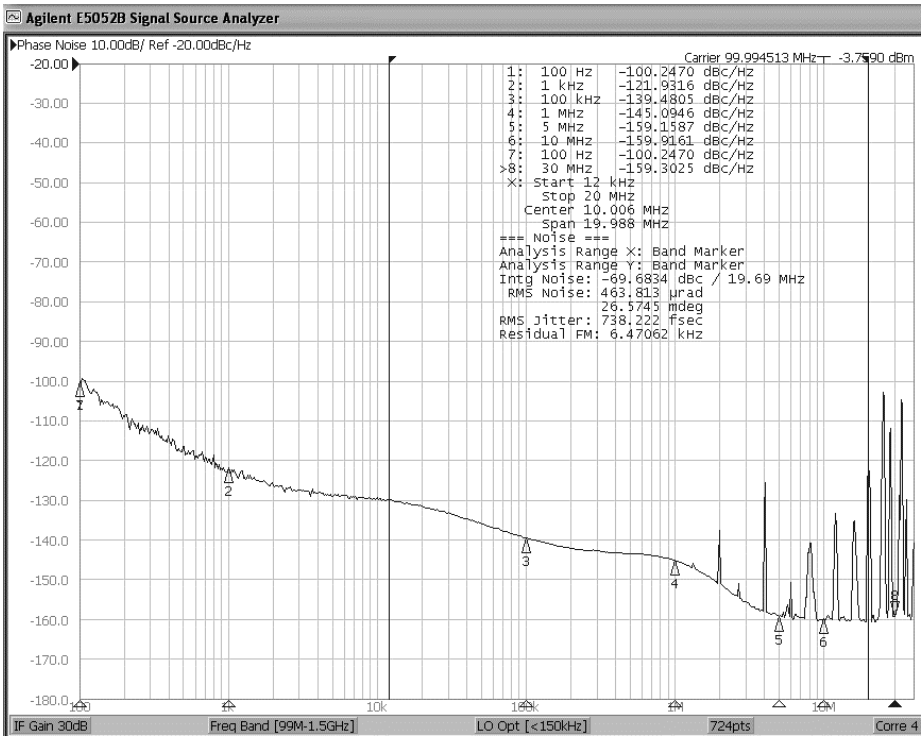
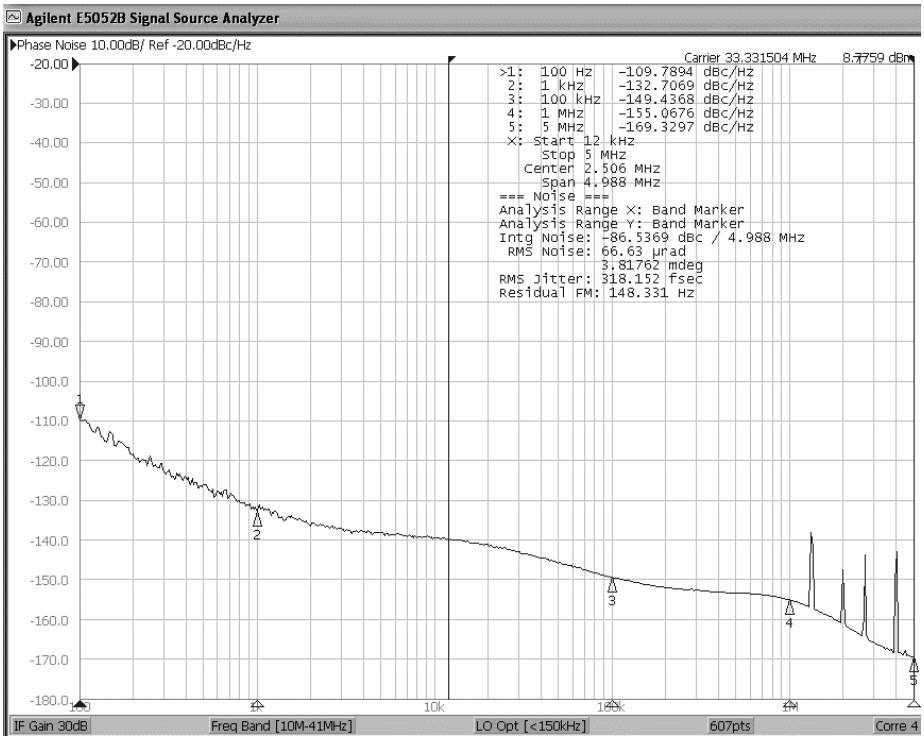
Phase Noise



100MHz LVDS: 0.74ps Phase Jitter for 12KHz to 20MHz



33.33MHz LVCMOS: 0.32ps Phase Jitter for 12KHz to 5MHz

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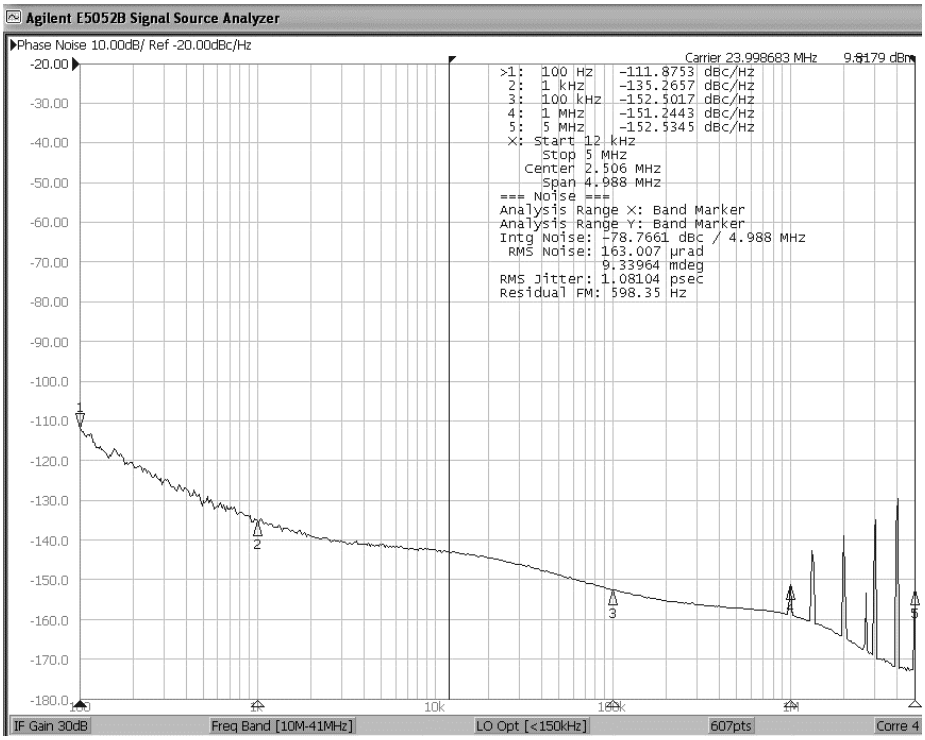
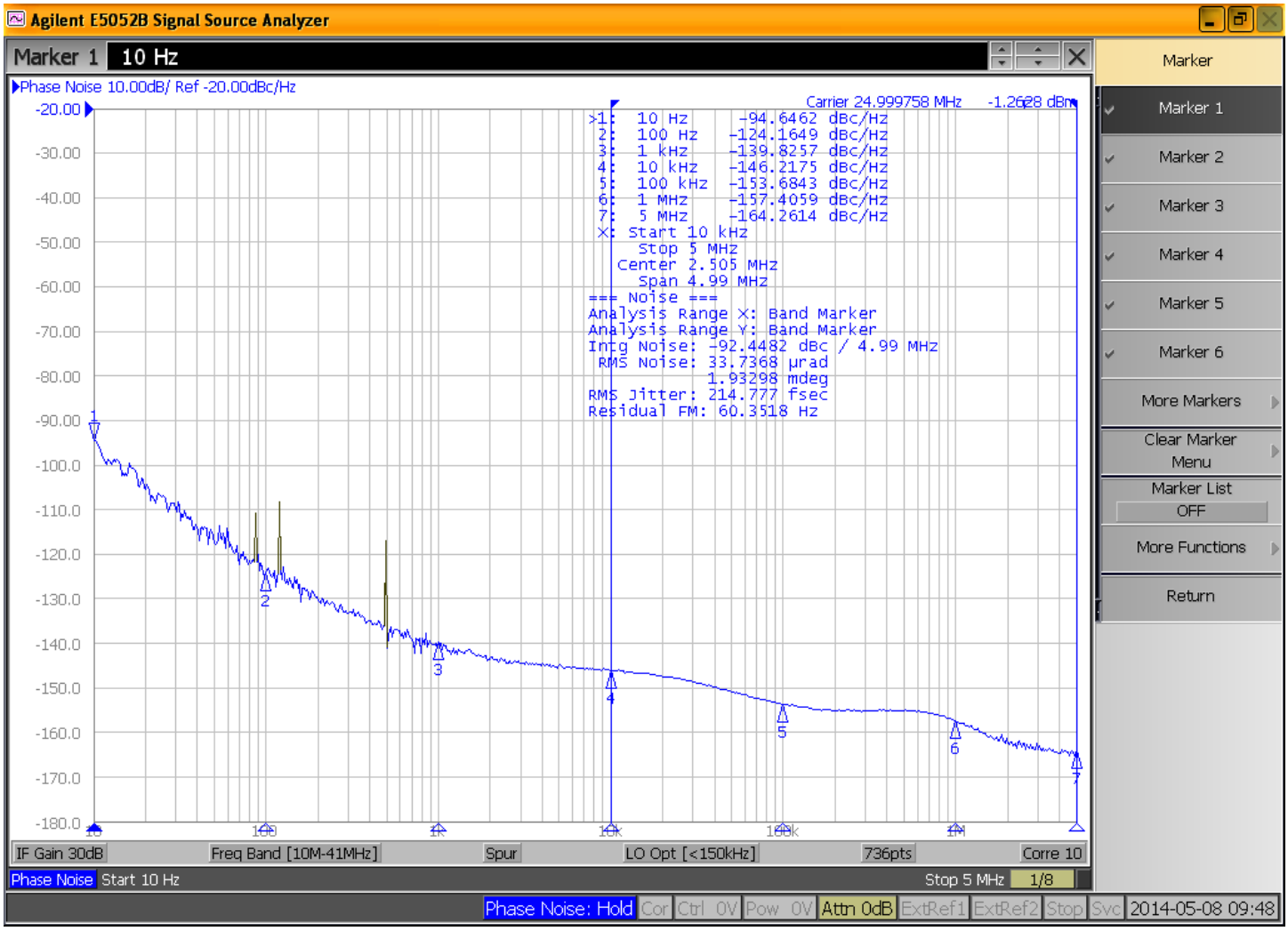
Phase Noise



24MHz LVCMOS: 1.1ps Phase Jitter for 12KHz to 5MHz



25MHz LVDS: 0.21ps Phase Jitter for 10KHz to 5MHz

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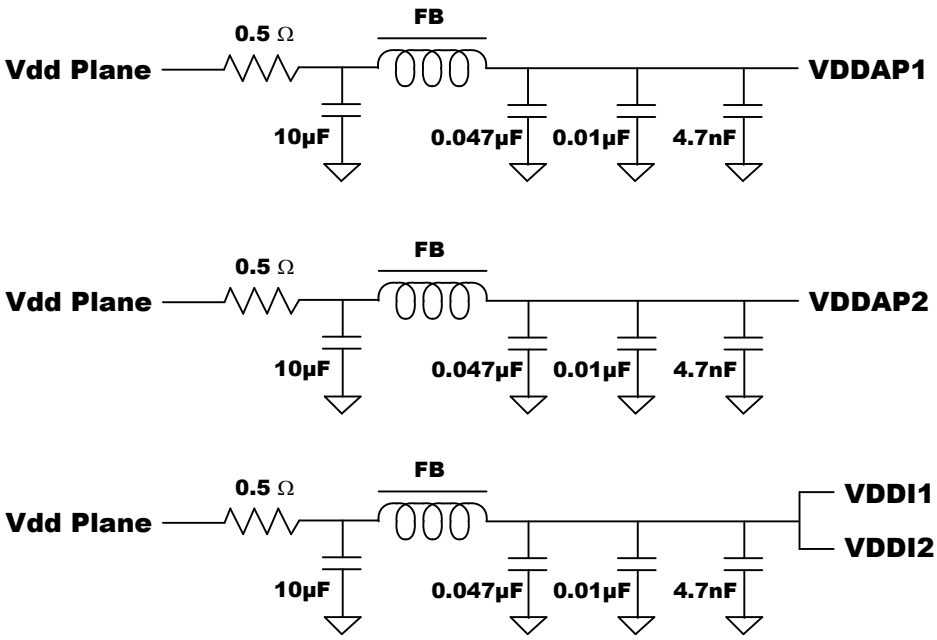
Power Supply Filtering Recommendations



- Use above power supply filtering for VDDAP1, VDDAP2, VDDI1 and VDDI2.
- Connect the VDDO and VDD pins directly to the VDD Power Plane.
- Connect all VSS pins directly to the Ground Power Plane.
- Connect the Thermal Relief Pad (Epad) directly to the Ground Power Plane, both for Electrical and Thermal reasons.
- Use Ferrite Beat (FB) with 300Ω or higher impedance.
- Certain Power Pin Names appear more than once on the package. Connect together for lower impedance power connection.

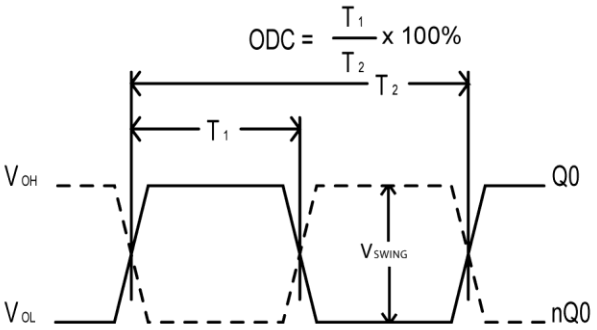


Figure 1. Duty Cycle Timing

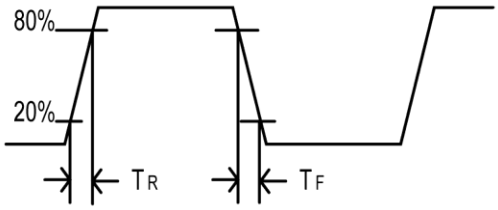


Figure 2. All Outputs Rise/Fall Time

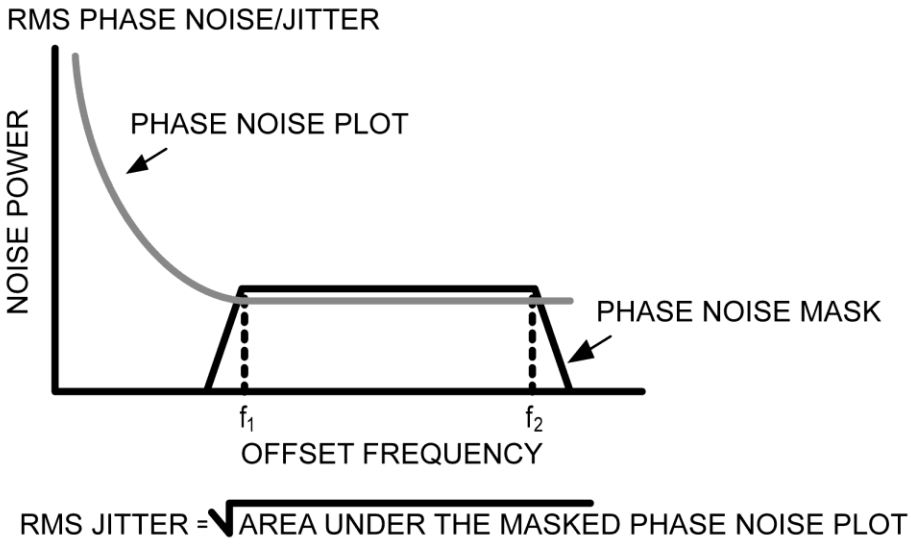


Figure 3. RMS Phase/Noise Jitter

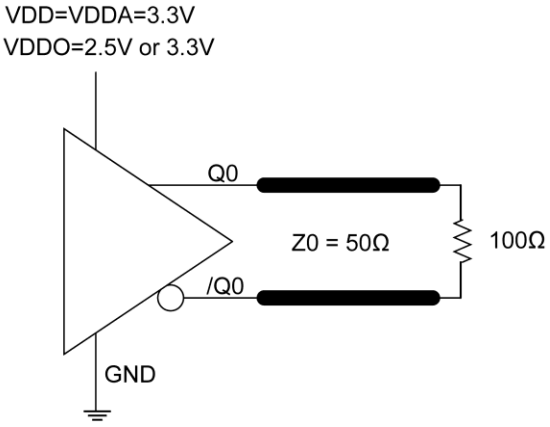


Figure 4. LVDS Output Load and Test Circuit

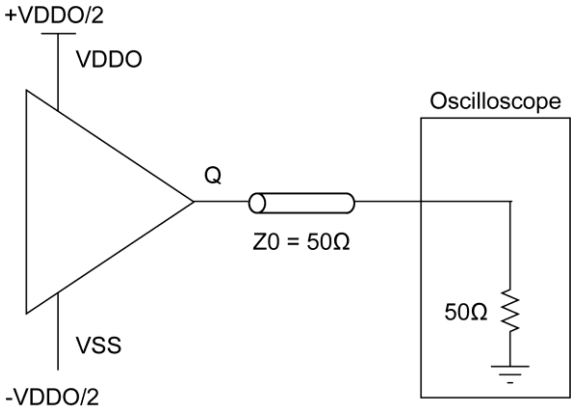


Figure 5. LVCMOS Output Load and Test Circuit

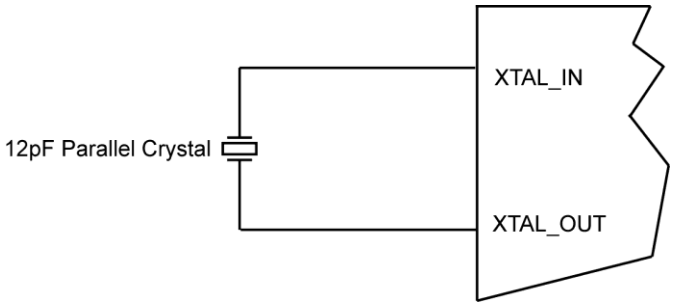


Figure 6. Crystal Input Interface

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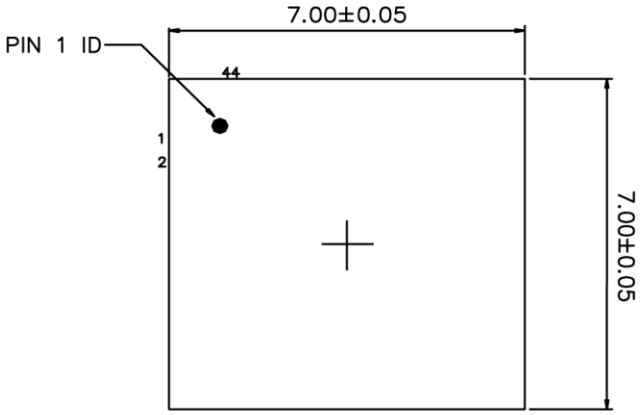
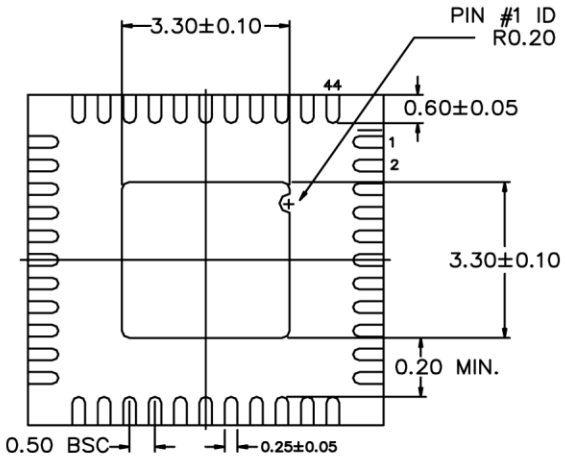
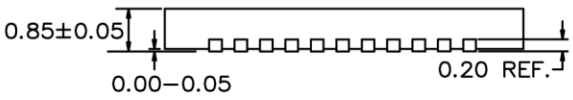
Package Information



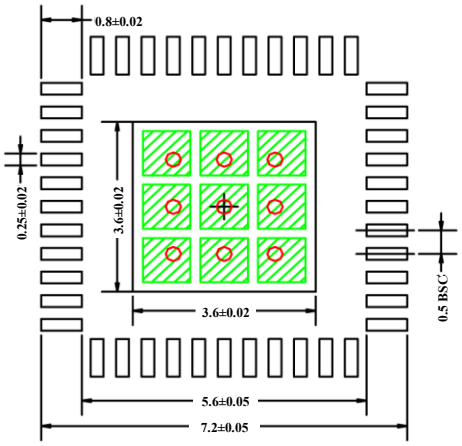
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30−0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.0MM PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93x0.93MM, SPACING IS 0.2MM

Note:
1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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Revision Template History

Date	Change Description/Edits by:	Rev.
8/12/2013	Initial draft. Copy from SM803025. / Eddy van Keulen	0.01
8/28/2013	Updated 44-pin package drawing	0.02
4/8/2014	Initial draft. Copy from SM803025. / Norman Hsu	0.03