SM806022

Flexible Ultra-Low Jitter Clock Generator

ClockWorks® FLEX

General Description

The SM806022 is a member of the ClockWorks® FLEX family of devices from Microchip and provides an extremely low-noise timing solution. It is based upon a unique PLL architecture that provides very-low phase noise.

The device operates from a 2.5V or 3.3V power supply.

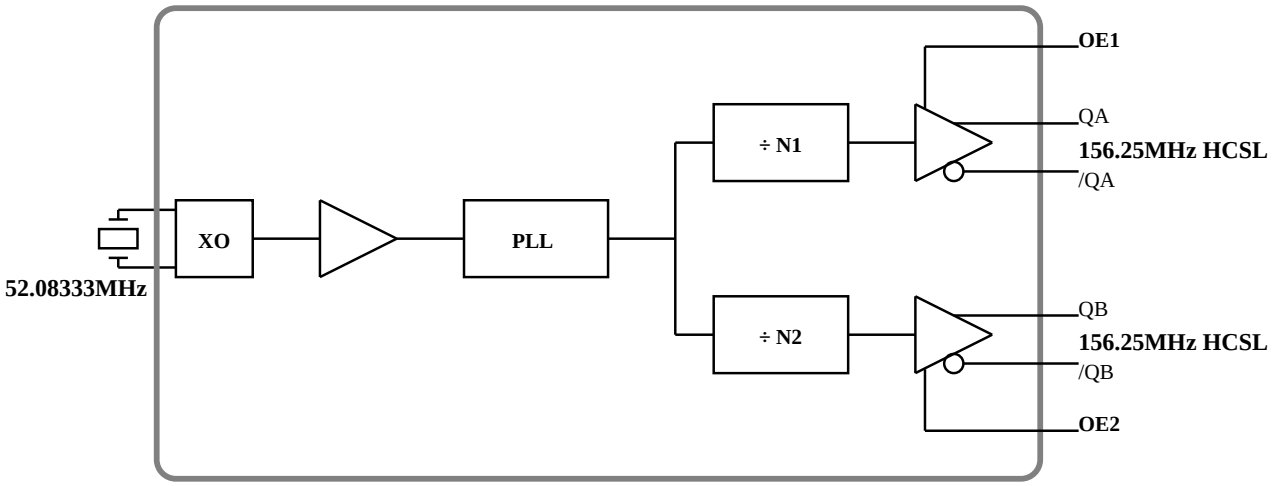
Applications

- 10/40/400 Gigabit Ethernet
- Fibre Channel 10G/12G SERDES

Features

- Generates 2 output clocks
- Frequency and output logic:
  - 156.25MHz HCSL x 2
- 52.08333MHz Crystal Input
- OE on banks A and B
- Typical phase noise:
  - 75fs (Integration range: 12kHz-20MHz)
- On-chip power supply regulation for excellent board level power supply noise immunity
- No external crystal oscillator capacitors required
- 2.5V or 3.3V operating power supply
- Industrial temperature range
- 24-Pin 4mm x 4mm QFN package

Block Diagram

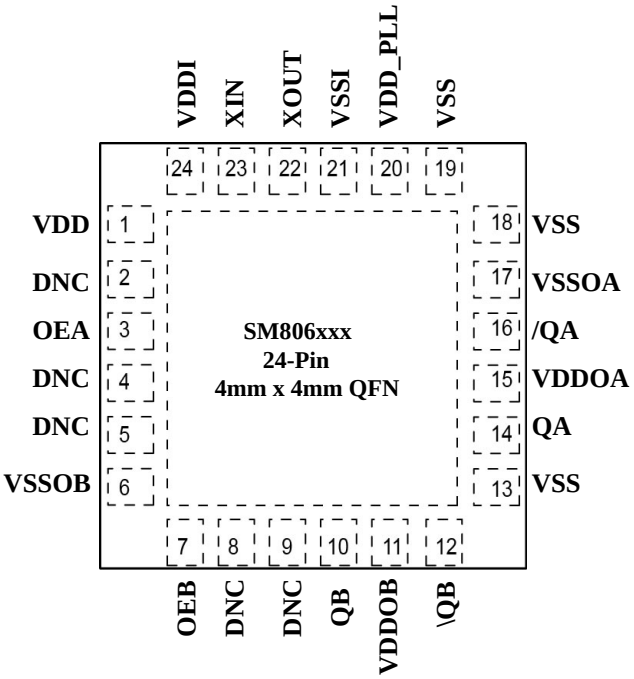


Ordering Information

Ordering Part Number	Marking	Shipping	Ambient Temperature Range	Package
SM806022UMG	806022	Tube	-40°C to +85°C	24-Pin QFN (4x4 mm)
SM806022UMG TR	806022	Tape and Reel	-40°C to +85°C	24-Pin QFN (4x4 mm)

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	VDD	PWR		Power Supply
2, 4, 5, 8, 9	DNC			Do not connect anything to these pins
3	OEA	I, SE	LVCMOS	Output Enable, QA outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up
6	VSSOB	PWR		Power Supply Return for QB Outputs
7	OEB	I, SE	LVCMOS	Output Enable, QB outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up
10, 12	QB, /QB	O, Diff	HCSL	Clock Output QB Frequency = 156.25MHz
11	VDDOB	PWR		Power Supply for QB Outputs
13, 18, 19	VSS	PWR		Core Power Supply Ground
14, 16	QA, /QA	O, Diff	HCSL	Clock Output QA Frequency = 156.25MHz
15	VDDOA	PWR		Power Supply for QA Outputs
17	VSSOA	PWR		Power Supply Return for QA Outputs
20	VDD_PLL	PWR		PLL Power
21	VSSI	PWR		I/O and XO Power Return
22, 23	XOUT, XIN	I/O, SE		Crystal Reference Input/Output = 52.08333MHz
24	VDDI	PWR		I/O and XO Power Supply

Absolute Maximum Ratings[1]

Supply Voltage (VDD, VDDA, VDDI, VDDO).....+4.6V
Input Voltage (VIN).....-0.50V to 4.6V
Lead Temperature (soldering, 20s).....260°C
Case Temperature.....115°C
Storage Temperature (T_S).....-65°C to +150°C
ESD Machine Model.....200V
ESD Human Body Model.....2000V

Operating Ratings[2]

Supply Voltage (VDD, VDDO)....+2.375V to +3.465V
Ambient Temperature (TA).....-40°C to +85°C
Junction Thermal Resistance
QFN (T_{JA}) Still Air.....24°C/W

DC Electrical Characteristics

Typical values are TA = 25°C, min/max across -40°C <= TA <= +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VDD, VDDO	Supply Voltage	2.5V Operation 3.3V Operation	2.375 3.135	2.5 3.3	2.625 3.465	V
VDDI1, VDDI2	Crystal XO & I/O Supply Voltage	2.5V Operation 3.3V Operation	2.375 3.135	2.5 3.3	2.625 3.465	V
VDDA	PLL Core Voltage		2.375		3.465	V
IDD_PLL	PLL Core Current Consumption			88	95	mA
IDDI	Analog Current Consumption			22	25	mA
IDDO	Output Stage Current Consumption			78	85	mA
IDD	SPI and Miscellaneous Logic			6	8	mA

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	8pF load typical	Fundamental, Parallel Resonant			
Frequency			52.08333		MHz
Equivalent Series Resistance (ESR)				60	Ohms
Load Capacitance, CL			8		pF
Shunt Capacitor, CO			1	3	pF
Correlation Drive Level			10	100	µW

Notes:
1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.

HCSL DC Electrical Characteristics

VDDcore= VDD = VDDO = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C, unless otherwise noted.
RL = 50 Ohms to VSS.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Output High Voltage		660	700	850	mV
VOL	Output Low Voltage		-150	0	27	mV
Vcross	Crossing Point Voltage			350		V

AC Electrical Characteristics

VDD = VDDO½ = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO½ = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
FIN	Input Frequency	XO		52.08333		MHz
FOUT	Output Frequency	HCSL		156.25 x 2		MHz
TR/TF	Output Rise/Fall time[3]	HCSL ouput	175	340	700	ps
ODC	Output Duty Cycle	<400MHz output frequencies	48	50	52	%
Tskew	Output-to-Output Skew	Notes 4, 5 Same output bank			50	ps
Tlock	PLL Lock Time			5	20	ms
Tjit(Ø)	RMS Phase Noise	Notes 6, 7 Integration range (12kHz-20MHz)		75		fs

Notes:
3. See Figure 'All Outputs Rise/Fall Time'
4. Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.
5. Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Measured using a 52.08333MHz crystal as the input reference source.

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *Quartz Crystals and Microchip ICs* application note ANTC207 for further details.
If you need help selecting a suitable crystal for your application, contact Microchip's TCG applications group at: tcghelp@microchip.com

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Filtering Recommendations

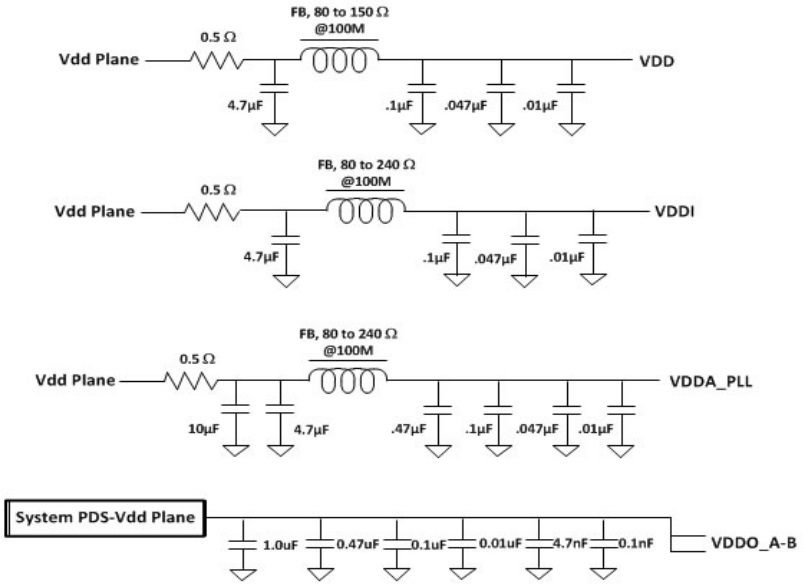


Figure 1. Recommended Power Supply Filtering

- Use the power supply filtering shown in above figure for VDD, VDDA_PLL, VDDI.
- Connect the VDDO pins directly to the VDD power plane.
- Connect all VSS pins directly to the ground power plane.
- Recommended ferrite bead properties are 80 Ohms to 240 Ohms @100MHz impedance and >250mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, Microchip's Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in below figure and can be used for any of the above VDD sections.
- Do not use Y5V or Z5U capacitors.

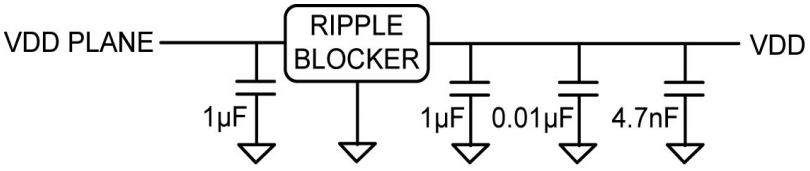


Figure 2. Power Supply Filtering with Ripple Blocker

Timing Diagrams

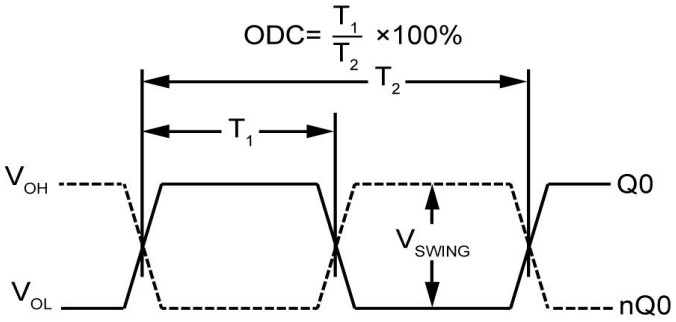


Figure 3. Duty Cycle Timing

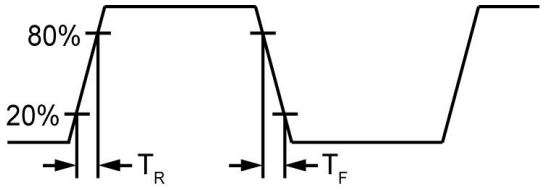


Figure 4. All Outputs Rise/Fall Time

RMS Phase/Noise/Jitter

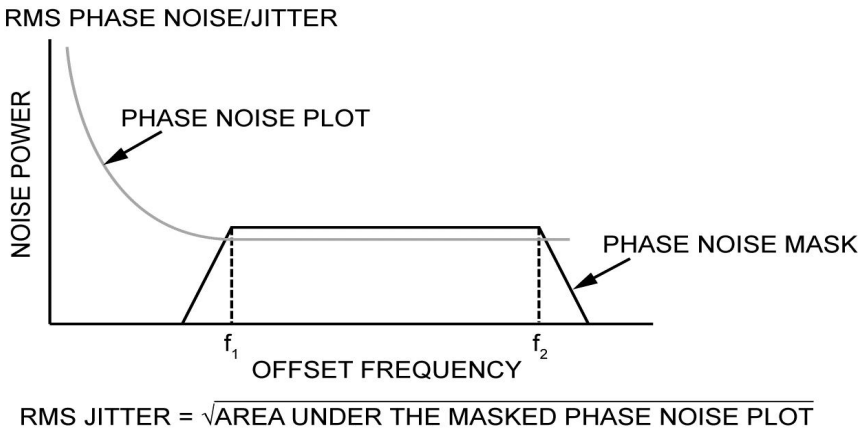


Figure 5. RMS Phase/Noise/Jitter

Crystal Input Interface

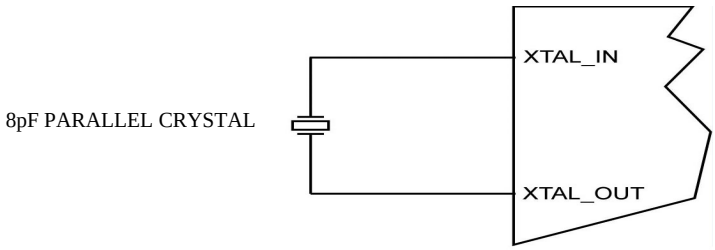


Figure 6. Crystal Input Interface

Output Termination

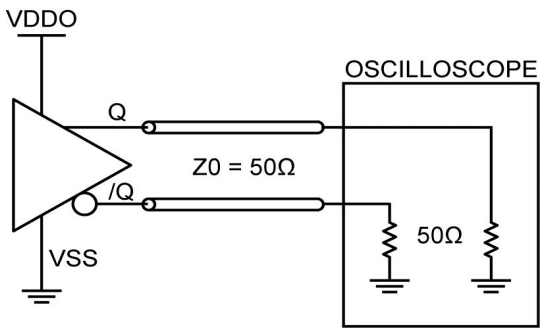


Figure 7. HCSL Output Load and Test Circuit

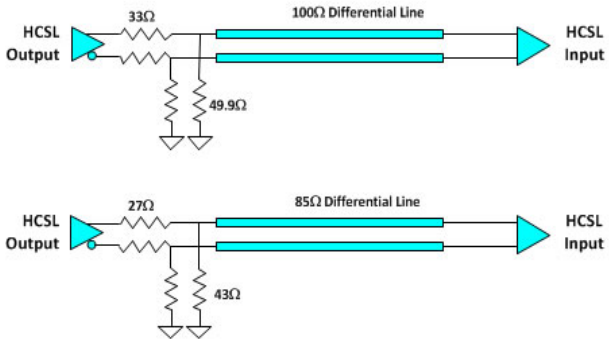


Figure 8. Recommended HCSL Output Termination Circuit

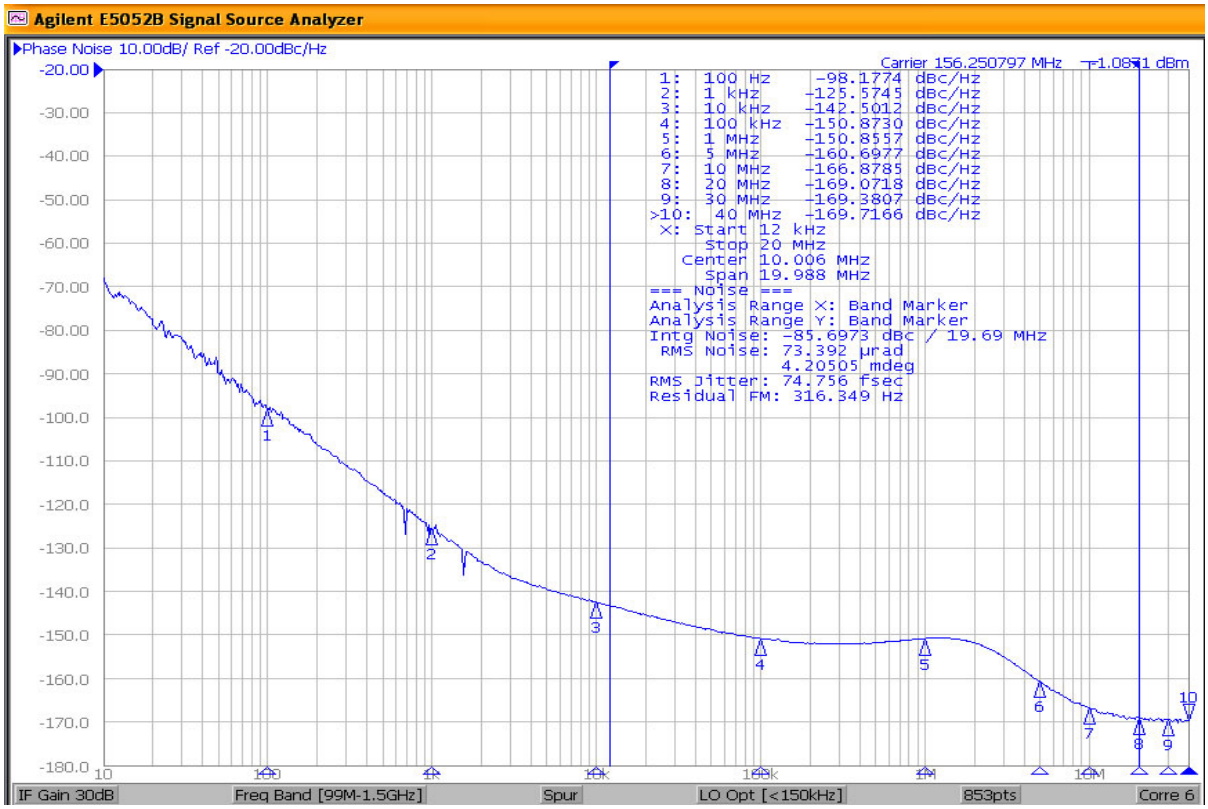
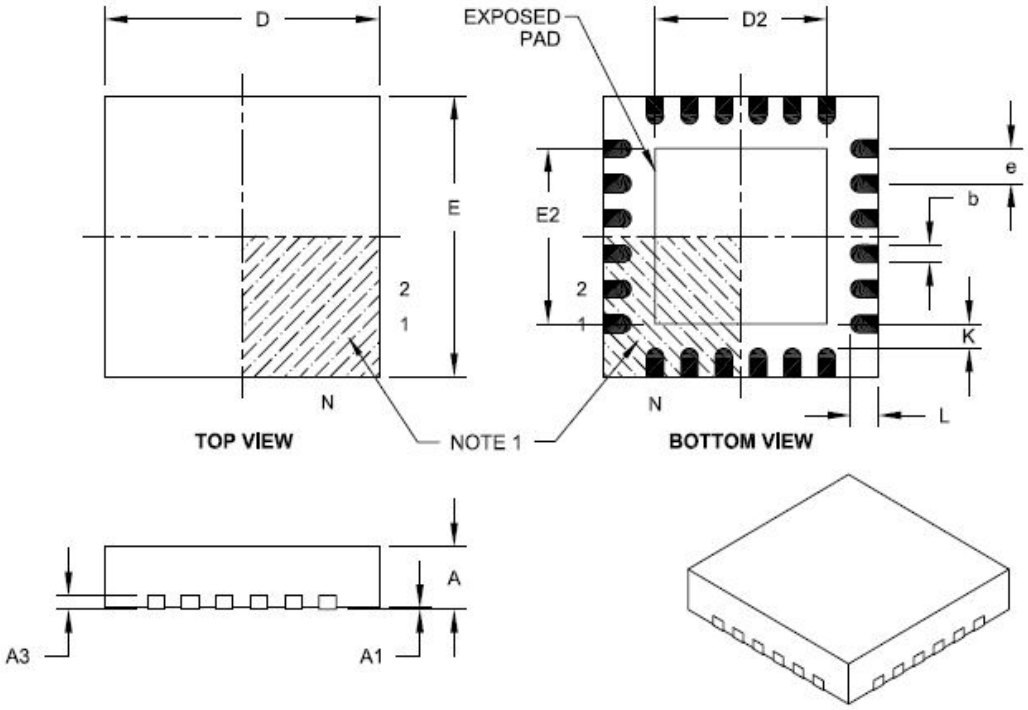


Figure 9. 156.25MHz HCSL Output, 12MHz-20MHz 75fs

24-Lead Plastic Quad Flat, No Lead Package (MJ) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.40	2.50	2.60
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.40	2.50	2.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

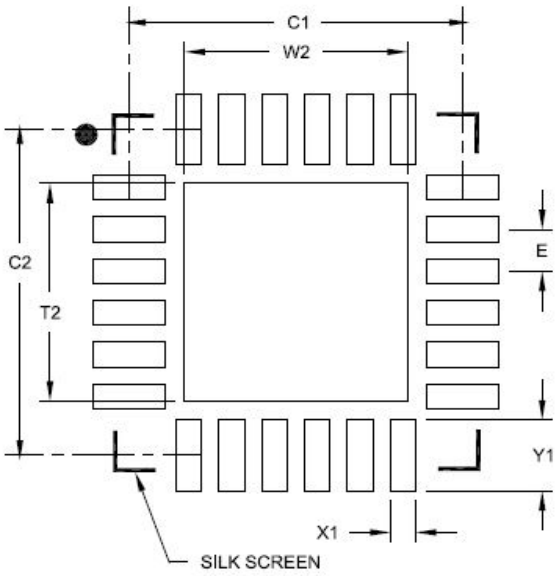
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-143A

24-Lead Plastic Quad Flat, No Lead Package (MJ) - 4x4 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.60
Optional Center Pad Length	T2			2.60
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.85

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2143B