# SM806048

## Flexible Ultra-Low Jitter Clock Generator

**ClockWorks® FLEX**

## General Description

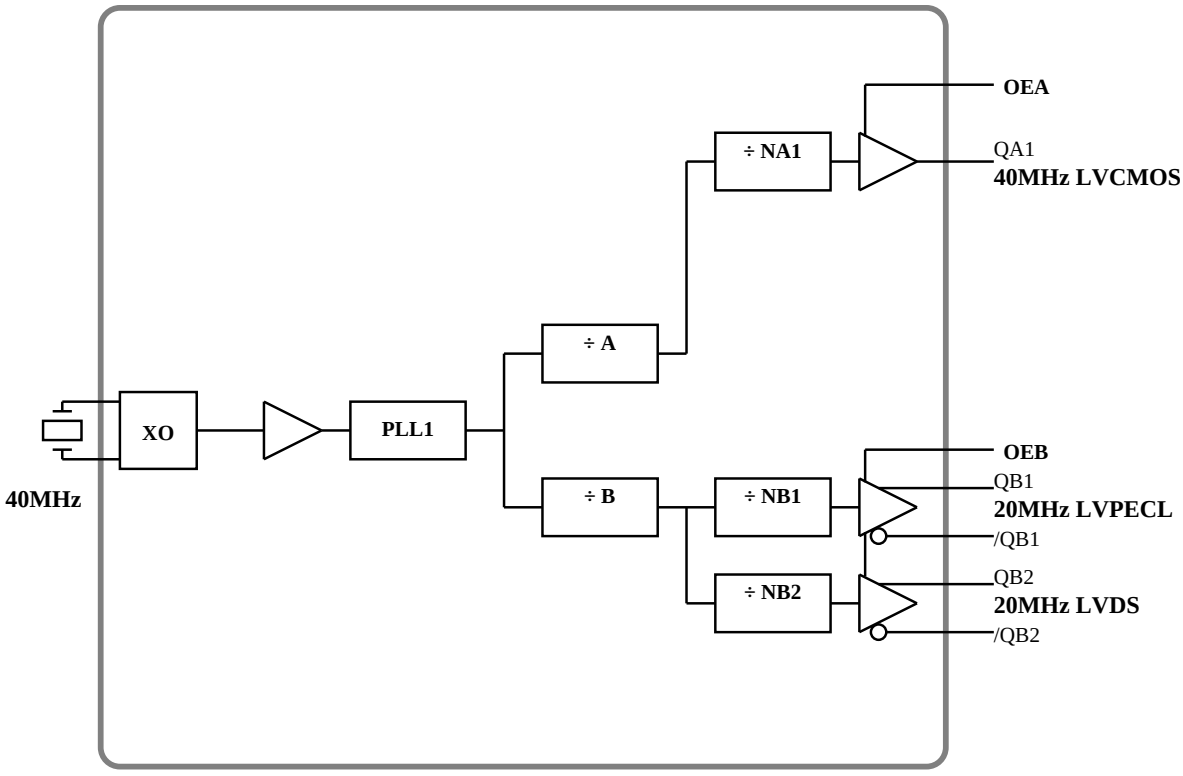
The SM806048 is a member of the ClockWorks® FLEX family of devices from Microchip and provides an extremely low-noise timing solution. It is based upon a unique PLL architecture that provides very-low phase noise.

The device operates from a 2.5V or 3.3V power supply.

## Features

- Generates 3 output clocks
- Frequency and output logic:
  - 40MHz LVCMOS x 1
  - 20MHz LVPECL x 1
  - 20MHz LVDS x 1
- 40MHz Crystal Input
- OE on banks A and B
- Typical phase noise:
  - 78fs (Integration range: 12kHz-20MHz)
- On-chip power supply regulation for excellent board level power supply noise immunity
- No external crystal oscillator capacitors required
- 2.5V or 3.3V operating power supply
- Industrial temperature range
- 48-pin 7x7x0.85mm VQFN

## Block Diagram

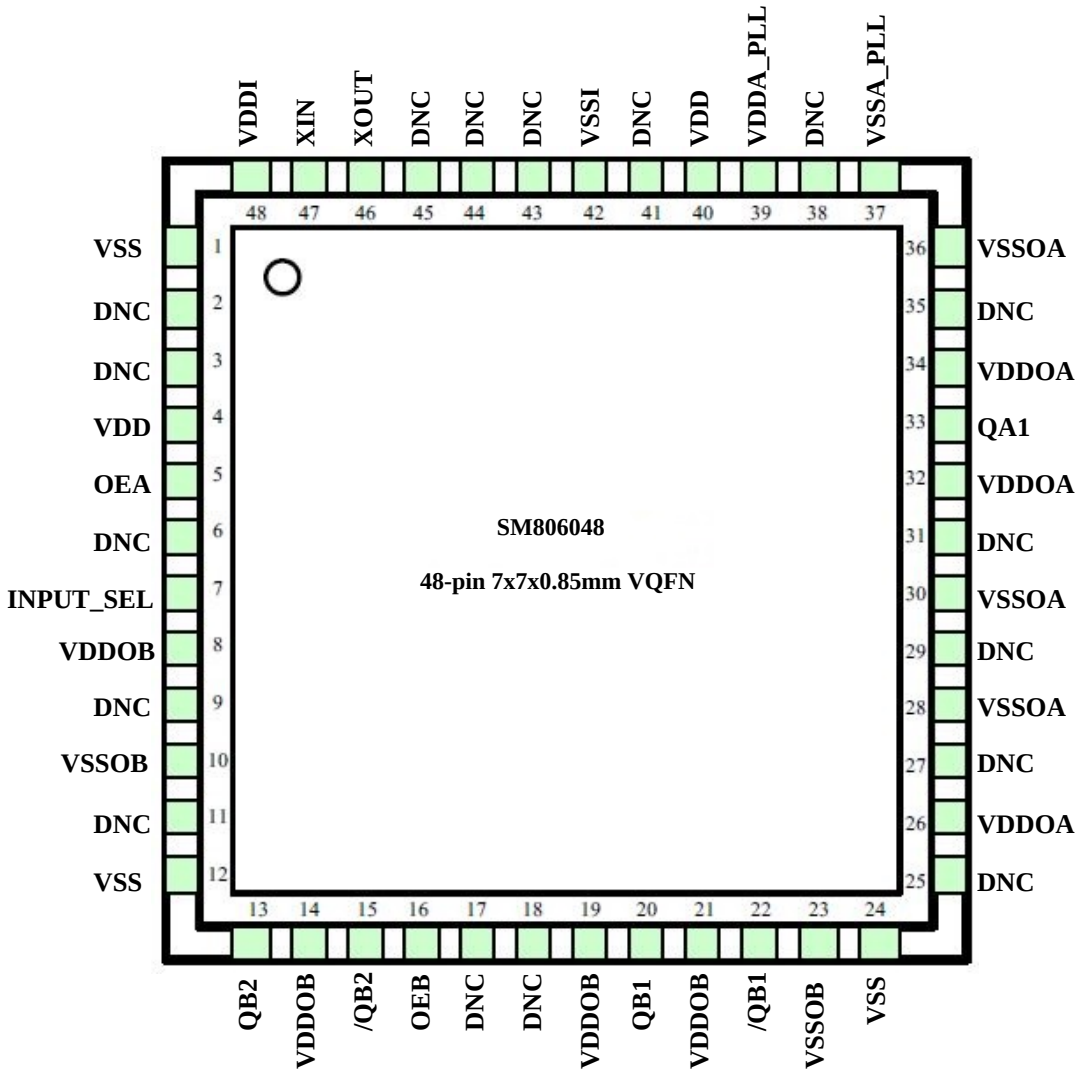


## Ordering Information

| Ordering Part Number | Marking | Shipping | Ambient Temperature Range | Package |
|---|---|---|---|---|
| SM806048UMG | 806048 | Tube | -40°C to +85°C | 48-pin 7x7x0.85mm VQFN |
| SM806048UMG TR | 806048 | Tape and Reel | -40°C to +85°C | 48-pin 7x7x0.85mm VQFN |

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

## Pin Configuration



## Pin Description

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Function |
|---|---|---|---|---|
| 1, 12, 24 | VSS | PWR | | Power Supply Ground |
| 2, 3, 6, 38, 41, 44 | DNC | | | Do not connect anything to these pins |
| 4 | VDD | PWR | | Power Supply |
| 5 | OEA | I, SE | LVCMOS | Output Enable, QA outputs disable to tri-state,<br>0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up |
| 7 | INPUT_SEL | I, SE | LVCMOS | Internal 75k Ohms Pull-Up<br>0 = REF_IN, 1 = XTAL |
| 8, 14, 19, 21 | VDDOB | PWR | | Power Supply for Outputs QB |
| 9, 11 | DNC, DNC | | | Do not conncet |
| 10, 23 | VSSOB | PWR | | Ground Return Path for the Bank B Output Drivers |
| 13, 15 | QB2, /QB2 | O, Diff | LVDS | Clock Output QB2 Frequency = 20MHz |
| 16 | OEB | I, SE | LVCMOS | Output Enable, QB outputs disable to tri-state,<br>0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up |
| 17 | DNC | | | Do not connect |
| 18 | DNC | | | Do not connect |
| 20, 22 | QB1, /QB1 | O, Diff | LVPECL | Clock Output QB1 Frequency = 20MHz |
| 25, 27 | DNC, DNC | | | Do not conncet |
| 26, 32, 34 | VDDOA | PWR | | Power Supply for Outputs QA |
| 28, 30, 36 | VSSOA | PWR | | Ground Return Path for the Bank A Output Drivers |
| 29, 31 | DNC, DNC | | | Do not conncet |
| 33, 35 | QA1, DNC | O, SE | LVCMOS | Clock Output QA1 Frequency = 40MHz |
| 37 | VSSA_PLL | PWR | | Analog Power Return for PLL |
| 39 | VDDA_PLL | PWR | | Analog Power Supply for PLL |
| 40 | VDD | PWR | | Power Supply |
| 42 | VSSI | PWR | | Ground for Reference Input Circuits and Crystal Oscillator |
| 43, 45 | DNC | | | Do not connect |
| 46, 47 | XOUT, XIN | I/O, SE | | Crystal Reference Input/Output = 40MHz,<br>no external load caps needed. |
| 48 | VDDI | PWR | | Power Supply for Reference Input Circuits and Crystal Oscillator |

## Absolute Maximum Ratings[1]

Supply Voltage (VDD, VDDA, VDDI, VDDO).....+4.6V
Input Voltage (VIN).....-0.50V to +4.6V
ESD Machine Model.....200V
ESD Human Body Model.....2kV

## Operating Ratings[2]

Supply Voltage (VDD, VDDO)....+2.375V to +3.465V

## Electrical Characteristics

Typical values are TA = 25°C, min/max across -40°C <= TA <= +85°C, unless otherwise noted.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VDD, VDDO | Supply Voltage | 2.5V Operation<br>3.3V Operation | 2.375<br>3.135 | 2.5<br>3.3 | 2.625<br>3.465 | V |
| VDDI | Analog & I/O Supply | | 2.375 | | 3.465 | V |
| VDDA | PLL Core | | 2.375 | | 3.465 | V |
| IDDA | PLL Core Current Consumption | | | | 60 | mA |
| IDDI | Analog & I/O Current | | | | 20 | mA |
| IDDO | Output Stage Current Consumption | Per output bank, unloaded | | | 70 | mA |
| IDD | SPI and Miscellaneous Logic | | | | 8 | mA |

## Crystal Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental, Parallel Resonant | | | |
| Frequency | Note 3 | | 40 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 60 | Ohms |
| Load Capacitance, CL | 8.0 pF parallel load, typical | | 8 | ±0.5 | pF |
| Shunt Capacitor, CO | | | 0.3 | 1.5 | pF |
| Correlation Drive Level | EIA-512 | | 10 | 200 | µW |

**Notes:**
1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.

## LVPECL DC Electrical Characteristics

VDDcore= VDD = VDDO = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C, unless otherwise noted.
RL = 50 Ohms to VDDO - 2V.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VOH | Output High Voltage | 50 Ohms to VDDO - 2V | VDDO - 1.35 | VDDO - 1.01 | VDDO - 0.8 | V |
| VOL | Output Low Voltage | 50 Ohms to VDDO - 2V | VDDO - 2 | VDDO - 1.78 | VDDO - 1.6 | V |
| Vswing | Peak-to-Peak Output Voltage | Figure "Duty Cycle Timing" | 0.65 | 0.77 | 0.95 | V |

## LVDS DC Electrical Characteristics

VDDcore= VDD = VDDO = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C, unless otherwise noted.
RL = 100 Ohms between Q and /Q.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VOD | Differential Output Voltage | Figure "Duty Cycle Timing" | 245 | 350 | 454 | mV |
| VCM | Common Mode Voltage | | 1.125 | 1.2 | 1.375 | V |
| VOH | Output High Voltage | | 1.248 | 1.375 | 1.602 | V |
| VOL | Output Low Voltage | | 0.898 | 1.025 | 1.252 | V |

## LVCMOS DC Electrical Characteristics

VDDcore= VDD = VDDO = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C, unless otherwise noted.
RL = 50 Ohms to VDDO/2.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VOH | Output High Voltage | Highest drive (default) | VDD - 0.8 | | | V |
| VOL | Output Low Voltage | | | | 0.5 | V |
| VIH | Input High Voltage | | VDD - 0.7 | | VDD + 0.3 | V |
| VIL | Input Low Voltage | | VSS - 0.3 | | 0.3 x VDD | V |
| IIH | Input High Current | VDD = VIN = 3.465V | | | 5 | µA |
| IIL | Input Low Current | VDD = 3.465V, VIN = 0V | -150 | | | µA |

## AC Electrical Characteristics

VDD = VDDO½ = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO½ = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| FIN | Input Frequency | XO | | 40 | | MHz |
| FOUT | Output Frequency | LVPECL, LVDS, LVCMOS | | 40 x 1<br>20 x 2 | | MHz |
| TR/TF | Output Rise/Fall time[3] | LVPECL ouput<br>LVDS ouput<br>LVCMOS ouput (default drive) | 85<br>85<br>100 | 135<br>140<br>200 | 350<br>300<br>400 | ps<br>ps<br>ps |
| ODC | Output Duty Cycle | <400MHz output frequencies | 48 | 50 | 52 | % |
| Tpd | Input-to-Input<br>Propagation Delay | ZDB mode<br>Generator/Bypass mode | -100 | <br>4 | 100 | ps<br>ns |
| Tskew | Output-to-Output Skew | Notes 4, 5<br>Same output bank | | | <br>50 | <br>ps |
| Tlock | PLL Lock Time | | | 5 | 20 | ms |
| Tjit(Ø) | RMS Phase Noise | Notes 6, 7<br>Integration range (12kHz-20MHz) | | <br>78 | | <br>fs |

## Temperature Specifications

| Parameter | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Ambient Temperature Range | Ta | -40 | | +85 | °C | |
| Lead Temperature | | | | +260 | °C | Soldering, 20s |
| Case Temperature | | | | +115 | °C | |
| Storage Temperature Range | Ts | -65 | | +150 | °C | |
| **Package Thermal Resistances (Note 8)** | | | | | | |
| Junction Thermal Resistance, 7 x 7 VQFN-48Ld | Tja | | 23.4 | | °C/W | |

**Notes:**
3. See Figure 'All Outputs Rise/Fall Time'
4. Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.
5. Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Measured using a 40MHz crystal as the input reference source.
8. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

## Application Information

### Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *Quartz Crystals and Microchip ICs* application note ANTC207 for further details.
If you need help selecting a suitable crystal for your application, contact Microchip's TCG applications group at: tcghelp@microchip.com

### Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

## Power Supply Filtering Recommendations

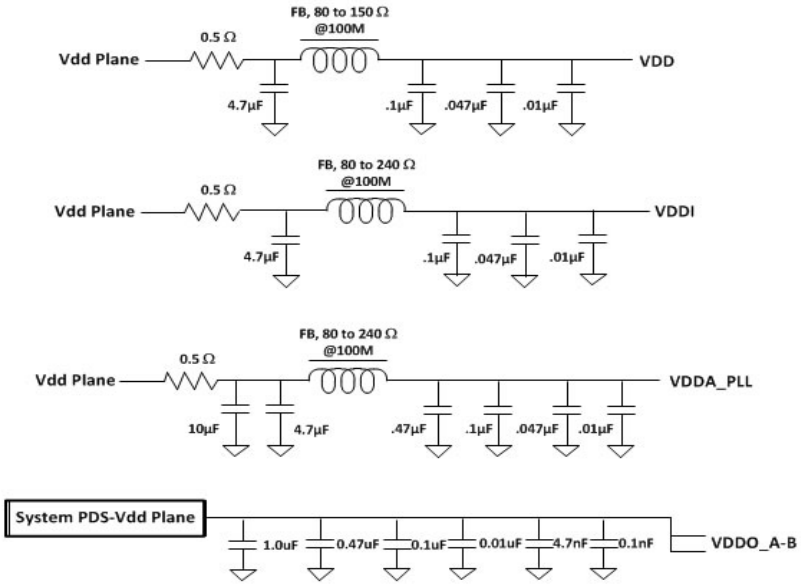



**Figure 1. Recommended Power Supply Filtering**

- Use the power supply filtering shown in above figure for VDD, VDDA_PLL, VDDI.
- Connect the VDDO pins directly to the VDD power plane.
- Connect all VSS pins directly to the ground power plane.
- Recommended ferrite bead properties are 80 Ohms to 240 Ohms @100MHz impedance and >250mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, Microchip's Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in below figure and can be used for any of the above VDD sections.
- Do not use Y5V or Z5U capacitors.

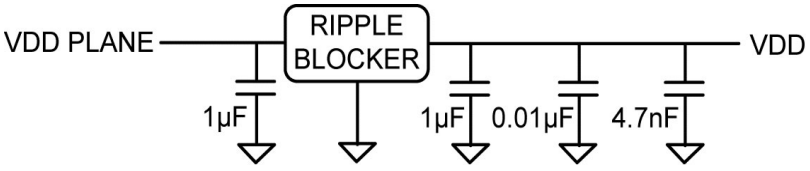



**Figure 2. Power Supply Filtering with Ripple Blocker**

## Timing Diagrams

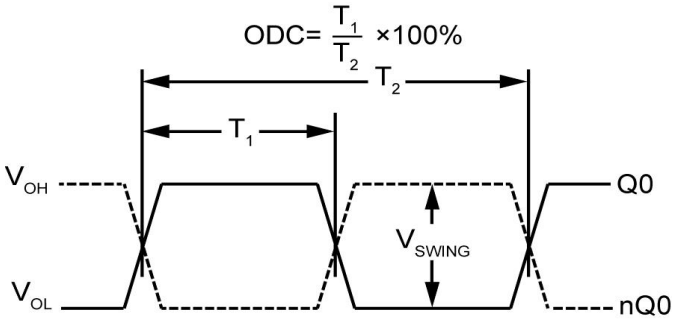



**Figure 3. Duty Cycle Timing**

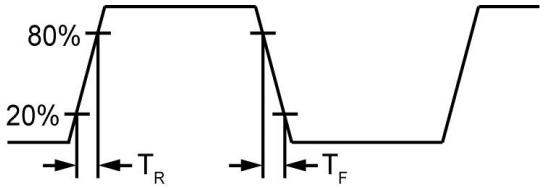



**Figure 4. All Outputs Rise/Fall Time**

## RMS Phase/Noise/Jitter

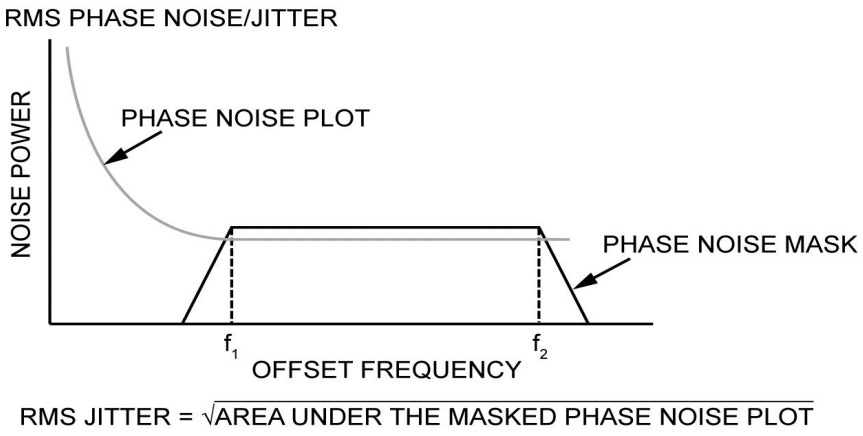



**Figure 5. RMS Phase/Noise/Jitter**

## Crystal Input Interface

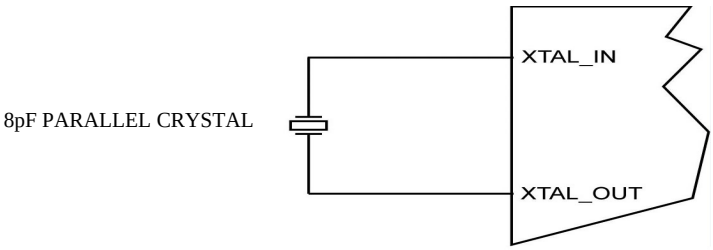



**Figure 6. Crystal Input Interface**

## Output Termination

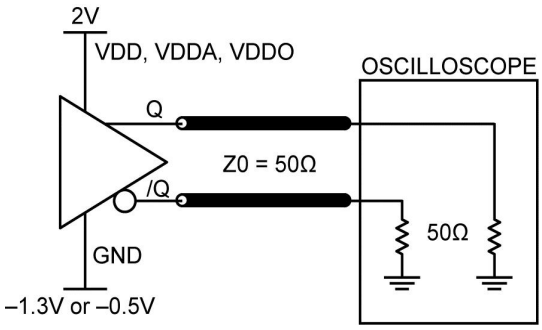



**Figure 7. LVPECL Output Load and Test Circuit**

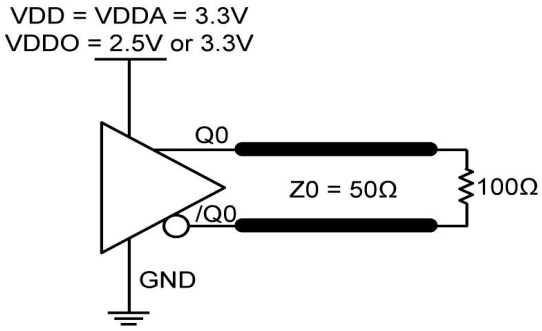



**Figure 8. LVDS Output Load and Test Circuit**

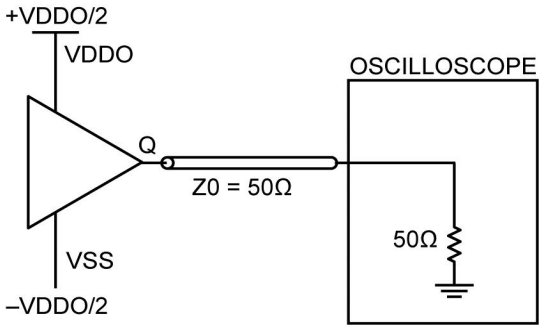
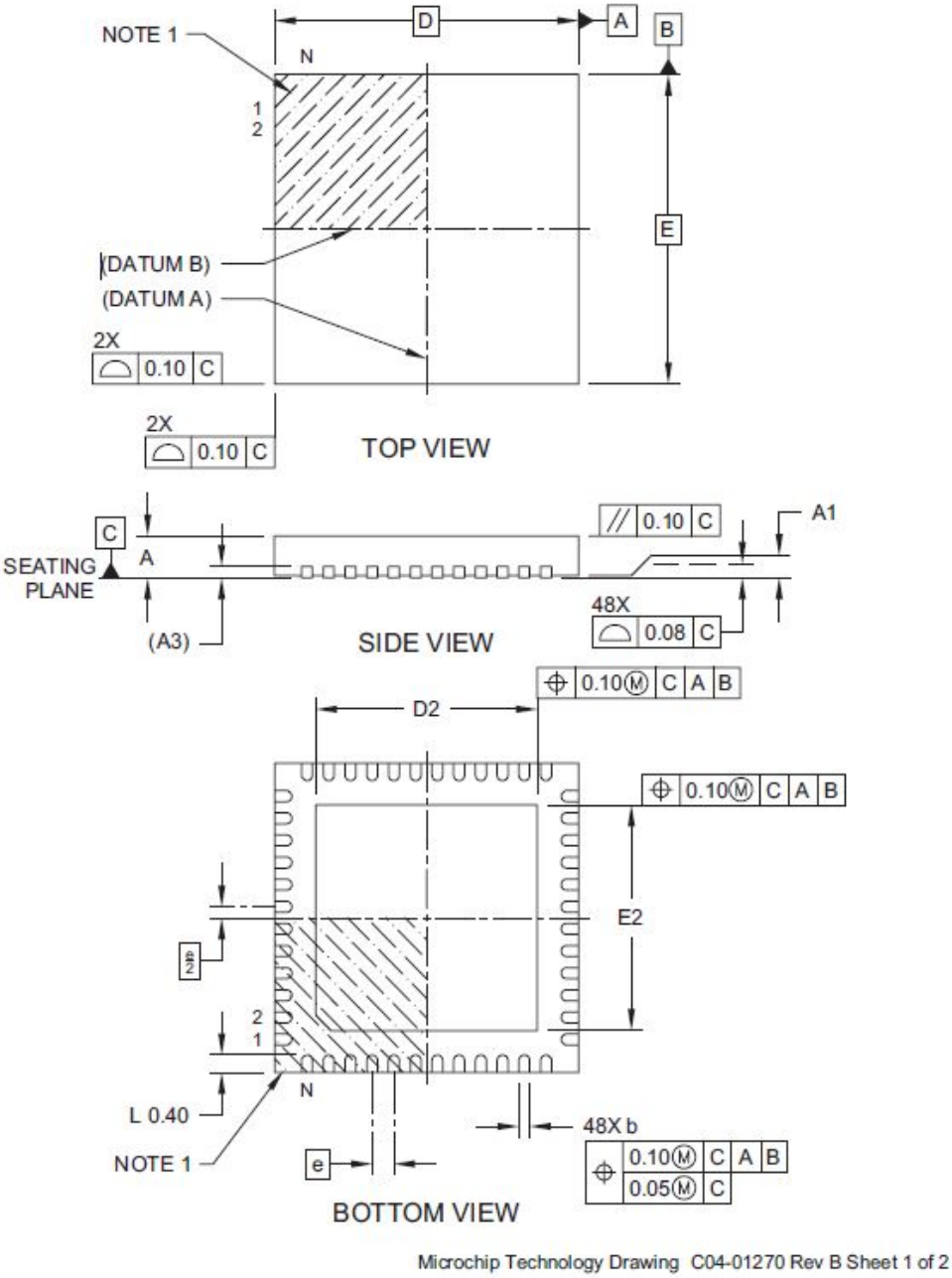



**Figure 9. LVCMOS Output Load and Test Circuit**

## Packaging Information

**48-Lead Very Thin Plastic Quad Flat, No Lead Package (PTA) - 7x7x0.9 mm Body [VQFN]**
**With 5.1x5.1 mm Exposed Pad; Micrel Legacy Package QFN77-48L**

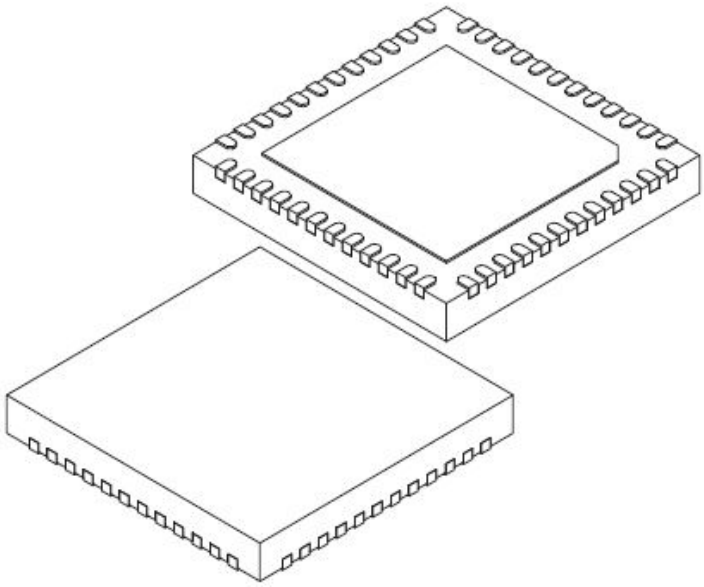
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-01270 Rev B Sheet 1 of 2

**48-Lead Very Thin Plastic Quad Flat, No Lead Package (PTA) - 7x7x0.9 mm Body [VQFN] With 5.1x5.1 mm Exposed Pad; Micrel Legacy Package QFN77-48L**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 48 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.253 REF | |
| Overall Length | D | | 7.00 BSC | |
| Exposed Pad Length | D2 | 5.05 | 5.10 | 5.15 |
| Overall Width | E | | 7.00 BSC | |
| Exposed Pad Width | E2 | 5.05 | 5.10 | 5.15 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.35 | 0.40 | 0.45 |

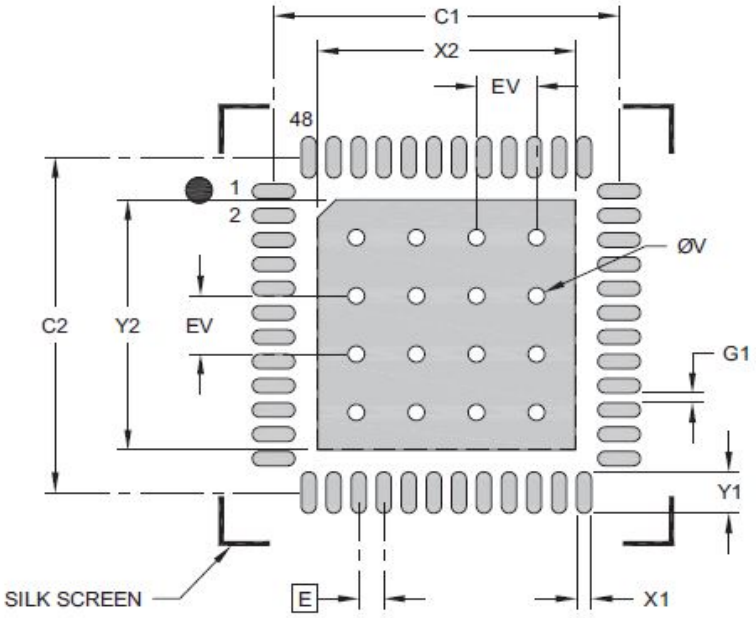
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-01270 Rev B Sheet 2 of 2

**48-Lead Very Thin Plastic Quad Flat, No Lead Package (PTA) - 7x7x0.9 mm Body [VQFN]**
**With 5.1x5.1 mm Exposed Pad; Micrel Legacy Package QFN77-48L**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 5.15 |
| Optional Center Pad Length | Y2 | | | 5.15 |
| Contact Pad Spacing | C1 | | 6.90 | |
| Contact Pad Spacing | C2 | | 6.90 | |
| Contact Pad Width (X48) | X1 | | | 0.30 |
| Contact Pad Length (X48) | Y1 | | | 0.85 |
| Contact Pad to Contact Pad (X44) | G1 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3270 Rev B