SM806073

Flexible Ultra-Low Jitter Clock Generator

ClockWorks® FLEX

General Description

The SM806073 is a member of the ClockWorks® FLEX family of devices from Microchip and provides an extremely low-noise timing solution. It is based upon a unique PLL architecture that provides very-low phase noise.

The device operates from a 2.5V or 3.3V power supply.

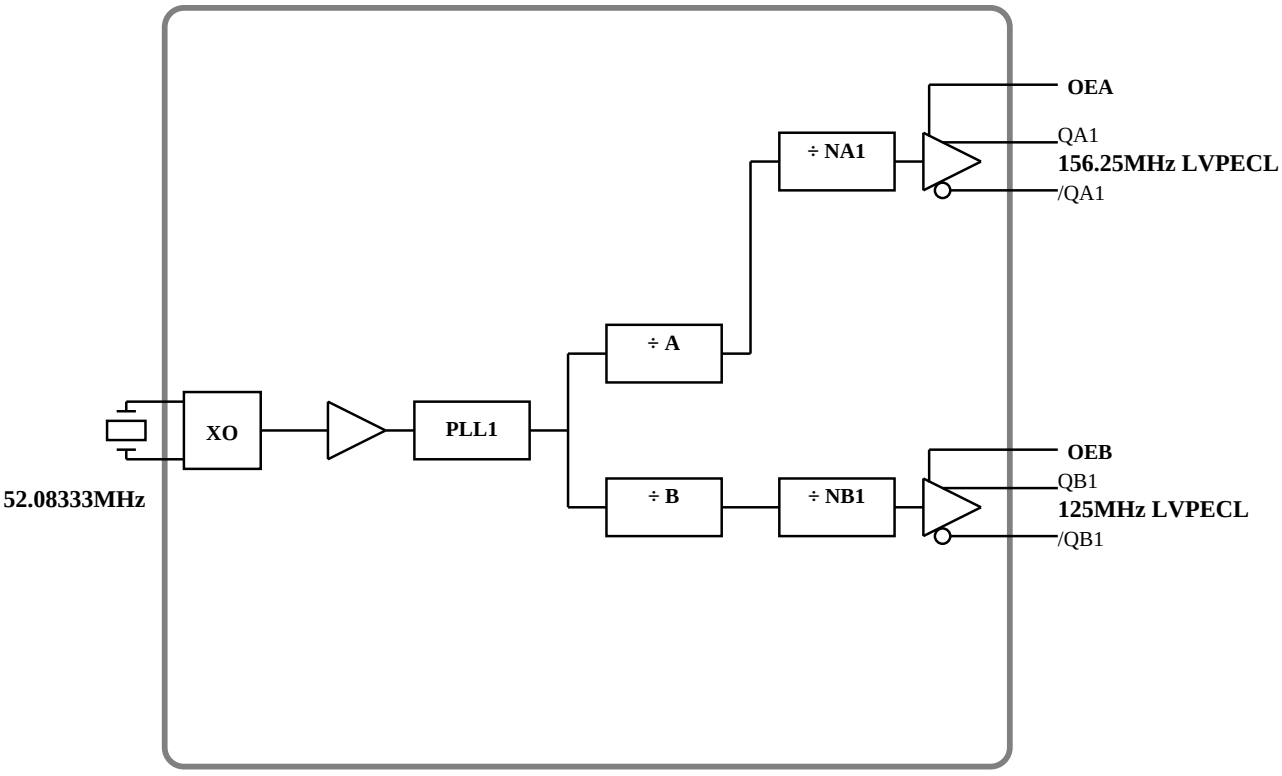
Applications

- Gigabit Ethernet
- 10/40/400 Gigabit Ethernet
- Storage
- Fibre Channel 10G/12G SERDES

Features

- Generates 2 output clocks
- Frequency and output logic:
  - 156.25MHz LVPECL x 1
  - 125MHz LVPECL x 1
- 52.08333MHz Crystal Input
- OE on banks A and B
- Typical phase noise:
  - 78fs (Integration range: 12kHz-20MHz)
- On-chip power supply regulation for excellent board level power supply noise immunity
- No external crystal oscillator capacitors required
- 2.5V or 3.3V operating power supply
- Industrial temperature range
- 24-pin 4x4x.85mm VQFN

Block Diagram

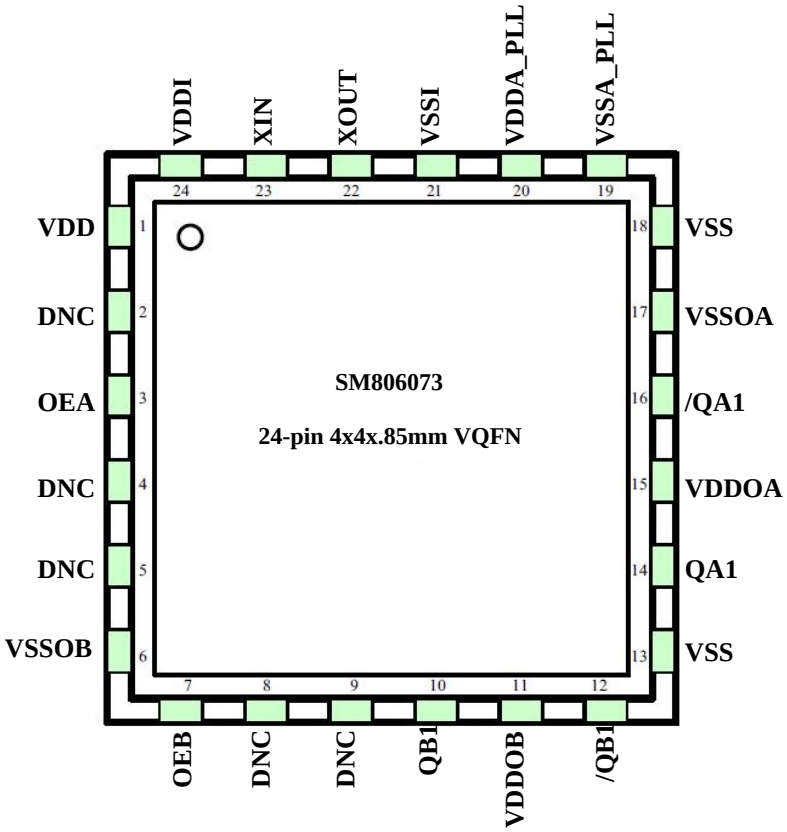


Ordering Information

Ordering Part Number	Marking	Shipping	Ambient Temperature Range	Package
SM806073UMG	806073	Tube	-40°C to +85°C	24-pin 4x4x.85mm VQFN
SM806073UMG TR	806073	Tape and Reel	-40°C to +85°C	24-pin 4x4x.85mm VQFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	VDD	PWR		Power Supply
2, 4, 5	DNC			Do not connect anything to these pins
3	OEA	I, SE	LVCMOS	Output Enable, QA outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up
6	VSSOB	PWR		Ground Return Path for the Bank B Output Drivers
7	OEB	I, SE	LVCMOS	Output Enable, QB outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75k Ohms Internal Pull-Up
8	DNC			Do not connect
9	DNC			Do not connect
10, 12	QB1, /QB1	O, Diff	LVPECL	Clock Output QB1 Frequency = 125MHz
11	VDDOB	PWR		Power Supply for Outputs QB
13, 18	VSS	PWR		Power Supply Ground
14, 16	QA1, /QA1	O, Diff	LVPECL	Clock Output QA1 Frequency = 156.25MHz
15	VDDOA	PWR		Power Supply for Outputs QA
17	VSSOA	PWR		Ground Return Path for the Bank A Output Drivers
19	VSSA_PLL	PWR		Analog Power Return for PLL
20	VDDA_PLL	PWR		Analog Power Supply for PLL
21	VSSI	PWR		Ground for Reference Input Circuits and Crystal Oscillator
22, 23	XOUT, XIN	I/O, SE		Crystal Reference Input/Output = 52.08333MHz, no external load caps needed.
24	VDDI	PWR		Power Supply for Reference Input Circuits and Crystal Oscillator

Absolute Maximum Ratings[1]

Supply Voltage (VDD, VDDA, VDDI, VDDO).....+4.6V
Input Voltage (VIN).....-0.50V to +4.6V
ESD Machine Model.....200V
ESD Human Body Model.....2kV

Operating Ratings[2]

Supply Voltage (VDD, VDDO)....+2.375V to +3.465V

Electrical Characteristics

Typical values are TA = 25°C, min/max across -40°C <= TA <= +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VDD, VDDO	Supply Voltage	2.5V Operation 3.3V Operation	2.375 3.135	2.5 3.3	2.625 3.465	V
VDDI	Analog & I/O Supply		2.375		3.465	V
VDDA	PLL Core		2.375		3.465	V
IDDA	PLL Core Current Consumption				60	mA
IDDI	Analog & I/O Current				20	mA
IDDO	Output Stage Current Consumption	Per output bank, unloaded			70	mA
IDD	SPI and Miscellaneous Logic				8	mA

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental, Parallel Resonant			
Frequency	Note 3		52.08333		MHz
Equivalent Series Resistance (ESR)				60	Ohms
Load Capacitance, CL	8.0 pF parallel load, typical		8	±0.5	pF
Shunt Capacitor, CO			0.3	1.5	pF
Correlation Drive Level	EIA-512		10	200	µW

Notes:
1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.

LVPECL DC Electrical Characteristics

VDDcore= VDD = VDDO = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C, unless otherwise noted.
RL = 50 Ohms to VDDO - 2V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Output High Voltage	50 Ohms to VDDO - 2V	VDDO - 1.35	VDDO - 1.01	VDDO - 0.8	V
VOL	Output Low Voltage	50 Ohms to VDDO - 2V	VDDO - 2	VDDO - 1.78	VDDO - 1.6	V
Vswing	Peak-to-Peak Output Voltage	Figure "Duty Cycle Timing"	0.65	0.77	0.95	V

AC Electrical Characteristics

VDD = VDDO½ = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO½ = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
FIN	Input Frequency	XO		52.08333		MHz
FOUT	Output Frequency	LVPECL		156.25 x 1 125 x 1		MHz
TR/TF	Output Rise/Fall time[3]	LVPECL ouput	85	135	350	ps
ODC	Output Duty Cycle	<400MHz output frequencies	48	50	52	%
Tpd	Input-to-Input Propagation Delay	ZDB mode Generator/Bypass mode	-100	 4	100	ps ns
Tskew	Output-to-Output Skew	Notes 4, 5 Same output bank			 50	 ps
Tlock	PLL Lock Time			5	20	ms
Tjit(Ø)	RMS Phase Noise	Notes 6, 7 Integration range (12kHz-20MHz)		 78		 fs

Temperature Specifications

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	Ta	-40		+85	°C	
Lead Temperature				+260	°C	Soldering, 20s
Case Temperature				+115	°C	
Storage Temperature Range	Ts	-65		+150	°C	
Package Thermal Resistances (Note 8)						
Junction Thermal Resistance, 4 x 4 VQFN-24Ld	Tja		25		°C/W	Still-Air

Notes:
3. See Figure 'All Outputs Rise/Fall Time'
4. Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.
5. Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Measured using a 52.08333MHz crystal as the input reference source.
8. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *Quartz Crystals and Microchip ICs* application note ANTC207 for further details.
If you need help selecting a suitable crystal for your application, contact Microchip's TCG applications group at: tcghelp@microchip.com

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Filtering Recommendations

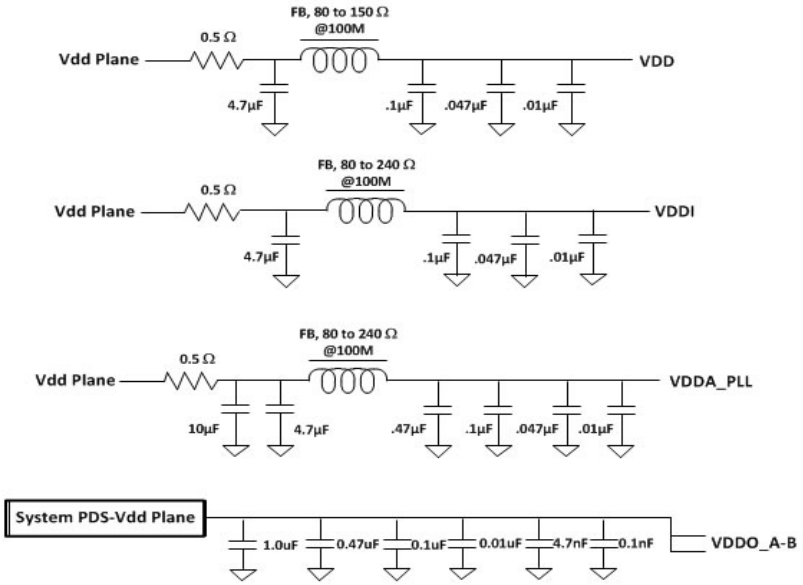


Figure 1. Recommended Power Supply Filtering

- Use the power supply filtering shown in above figure for VDD, VDDA_PLL, VDDI.
- Connect the VDDO pins directly to the VDD power plane.
- Connect all VSS pins directly to the ground power plane.
- Recommended ferrite bead properties are 80 Ohms to 240 Ohms @100MHz impedance and >250mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, Microchip's Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in below figure and can be used for any of the above VDD sections.
- Do not use Y5V or Z5U capacitors.

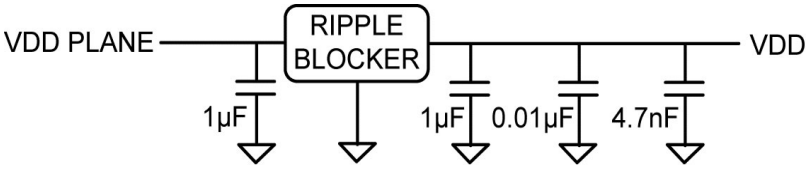


Figure 2. Power Supply Filtering with Ripple Blocker

Timing Diagrams

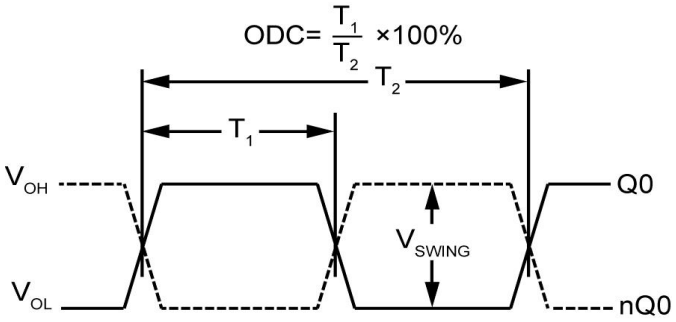


Figure 3. Duty Cycle Timing

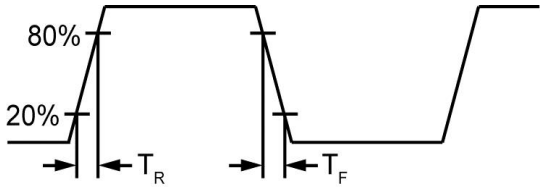


Figure 4. All Outputs Rise/Fall Time

RMS Phase/Noise/Jitter

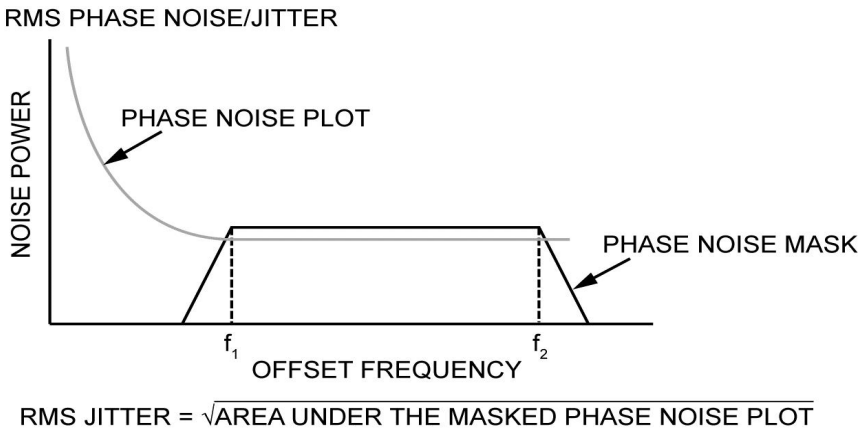


Figure 5. RMS Phase/Noise/Jitter

Crystal Input Interface

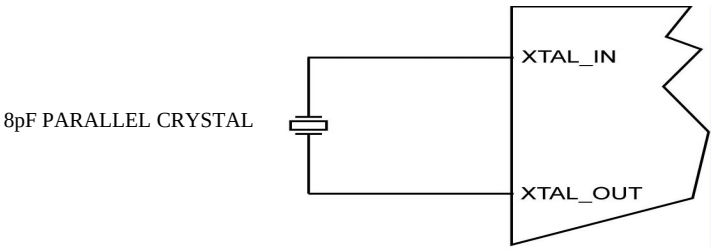


Figure 6. Crystal Input Interface

Output Termination

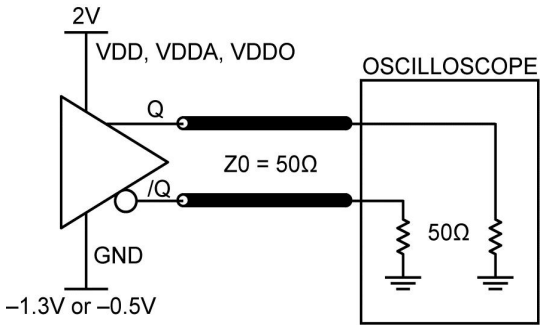
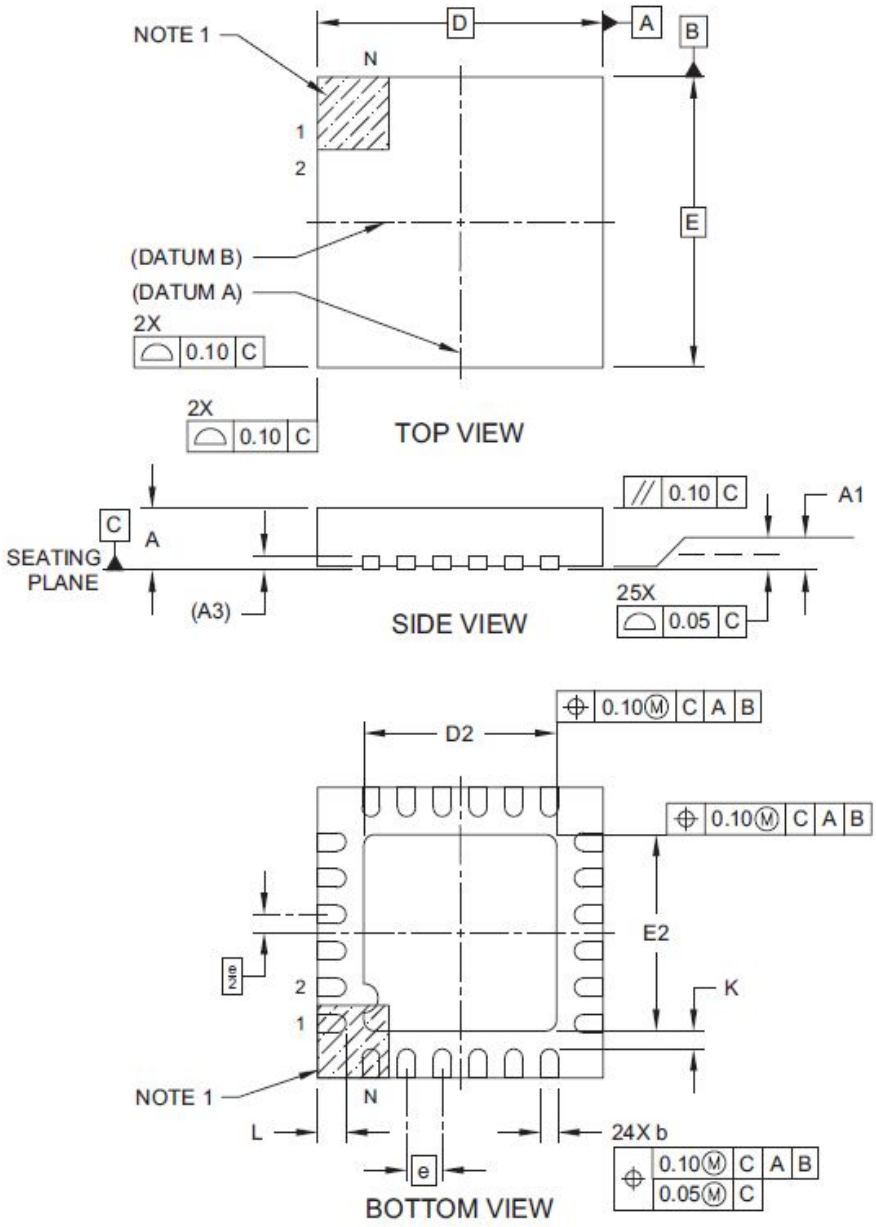


Figure 7. LVPECL Output Load and Test Circuit

Packaging Information

24-Lead Very Thin Plastic Quad Flat, No Lead Package (9KX) - 4x4 mm Body [VQFN]
With 2.7x2.7 mm Exposed Pad

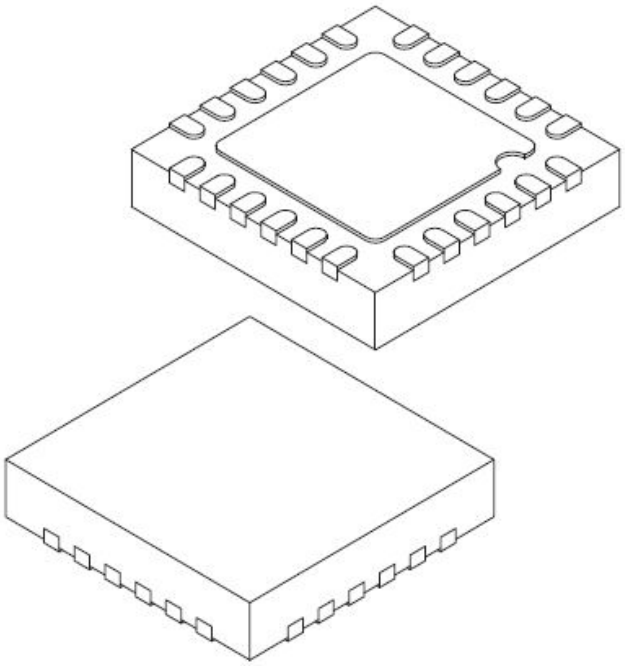
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-428 Rev A Sheet 1 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (9KX) - 4x4 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

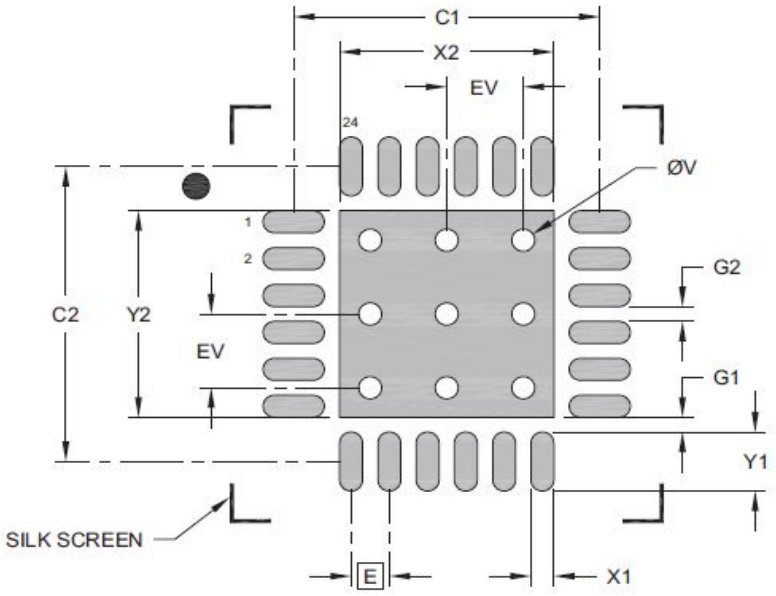
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-428 Rev A Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (9KX) - 4x4 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.80
Contact Pad to Center Pad (X24)	G1	0.20		
Contact Pad to Contact Pad (X20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2428 Rev A